RTU3B-2

A 1.0 V, 2.5 mW, Transformer Noise-Canceling UWB CMOS LNA

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RFIC – Atlanta June 15-17, 2008

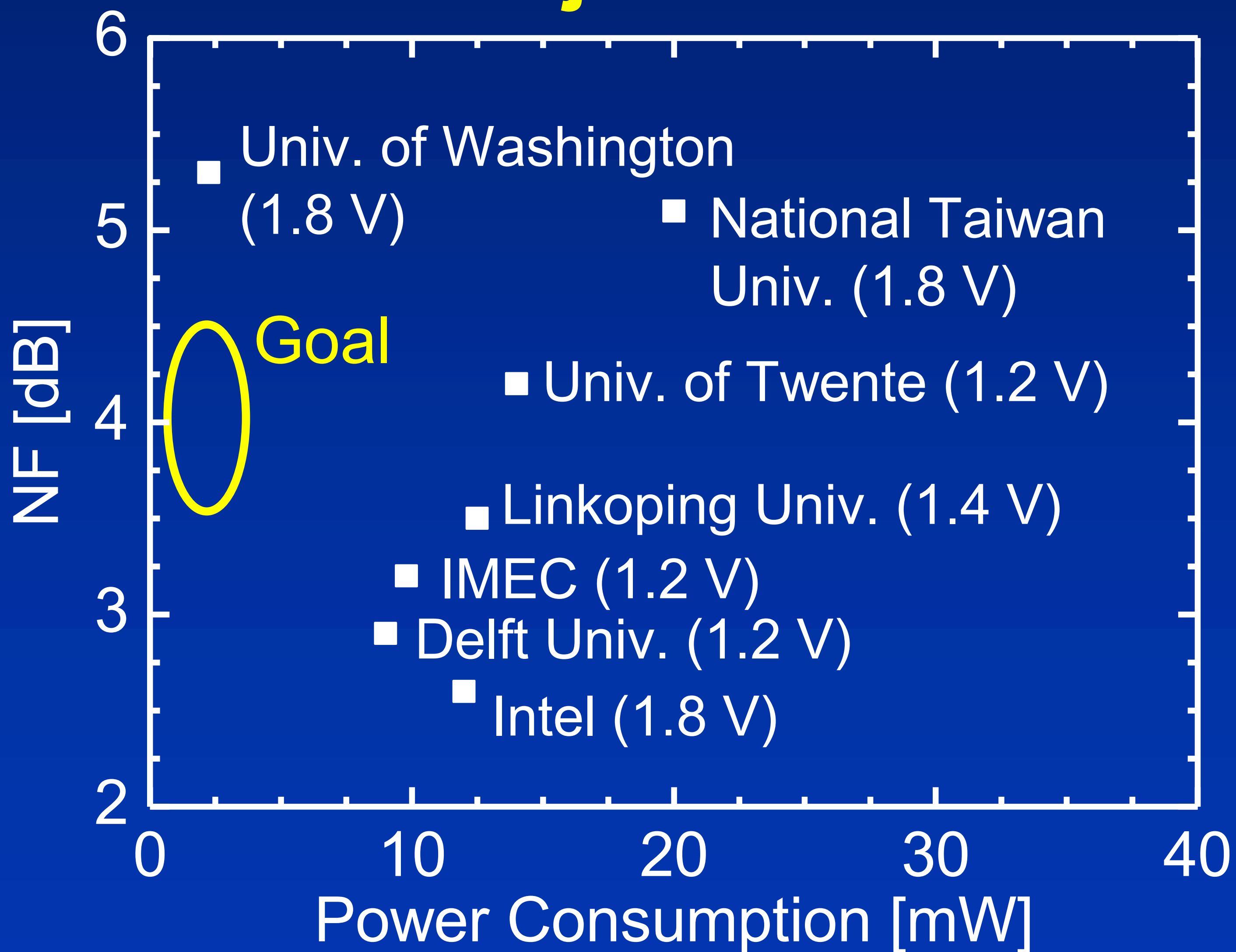
Outline

- Motivation and Objective
- Pros & Cons
- Transformer Noise-Canceling UWB LNA
  - Noise Cancellation Mechanisms
  - Wideband input Impedance Matching
- LNA Design
- Measurement Results
- Summary

Motivation

- Full-band (3.1–10.6 GHz) UWB receivers are desired
- Typical requirements for UWB LNAs:
  - S_{11}<-10 dB
  - S_{21} (voltage gain)>10 dB
  - NF<4 dB
- Previous wideband CMOS LNAs require:
  - High power consumption (about 10 mW)
  - High supply voltage (more than 1.2 V)

Objective



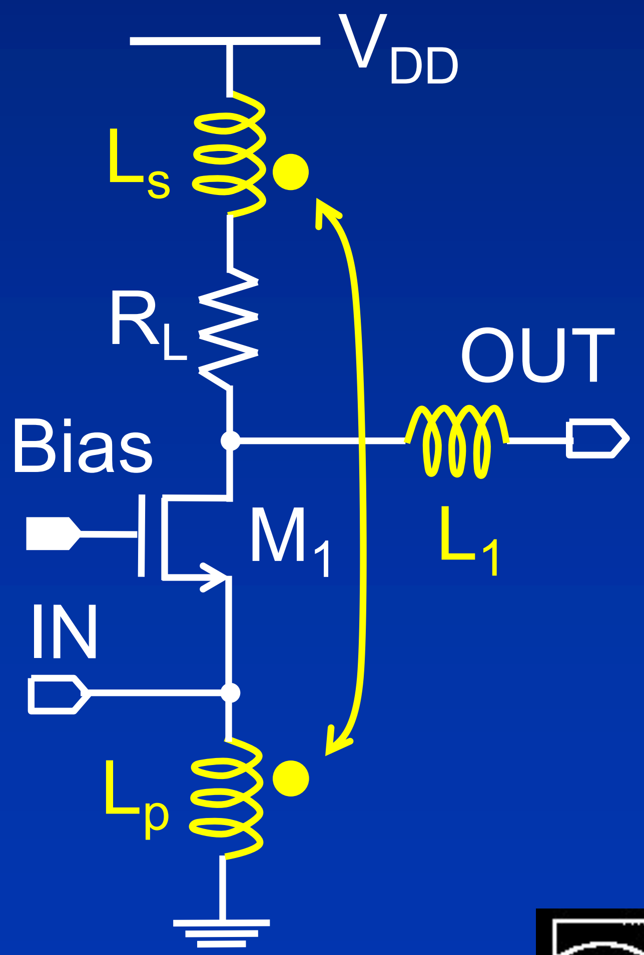
1.0 V, 2.5 mW, 4.0 dB NF, UWB CMOS LNA

Pros & Cons

- Pros:
  - Low power consumption (2.5 mW)
  - Low voltage operation (1.0 V)
- Cons:
  - Gain variation (3.8 dB across 3.1–10.6 GHz)

Transformer Noise-Canceling LNA

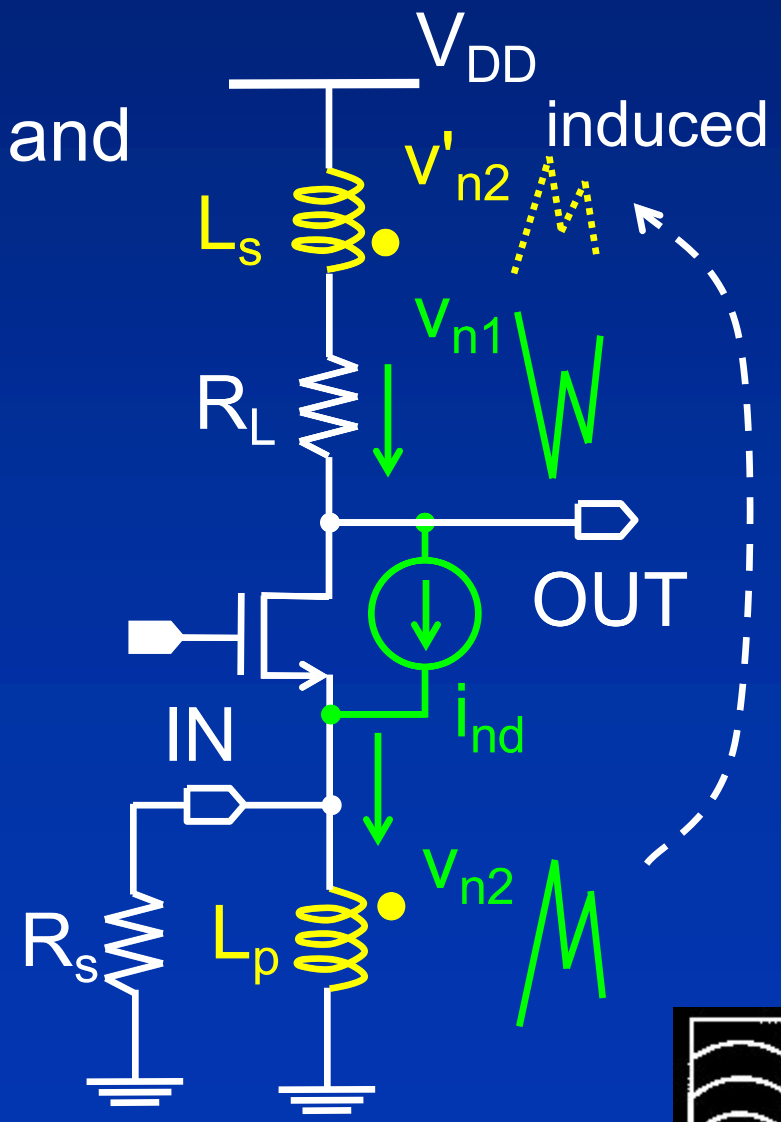
- The transformer partly cancels the noise of M_1 and R_L
- L_1 provides wideband input impedance matching
- Low-power and low-voltage operation



Noise Cancellation Mechanism (1)

1. i_{nd} flows through L_s and R_L, and generates v_{n1}
2. i_{nd} flows into L_p and R_s
3. The transformer detects i_{nd}, and induces v'_{n2}

The transformer reduces the effect of i_{nd}

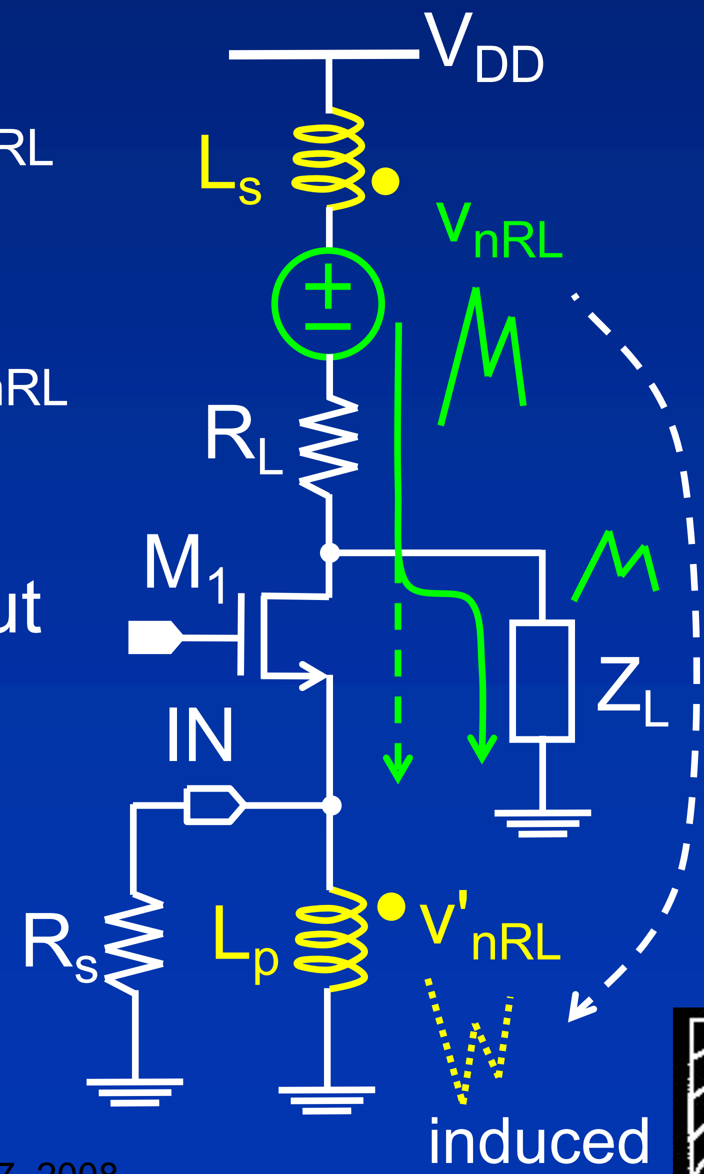


Noise Cancellation Mechanism (2)

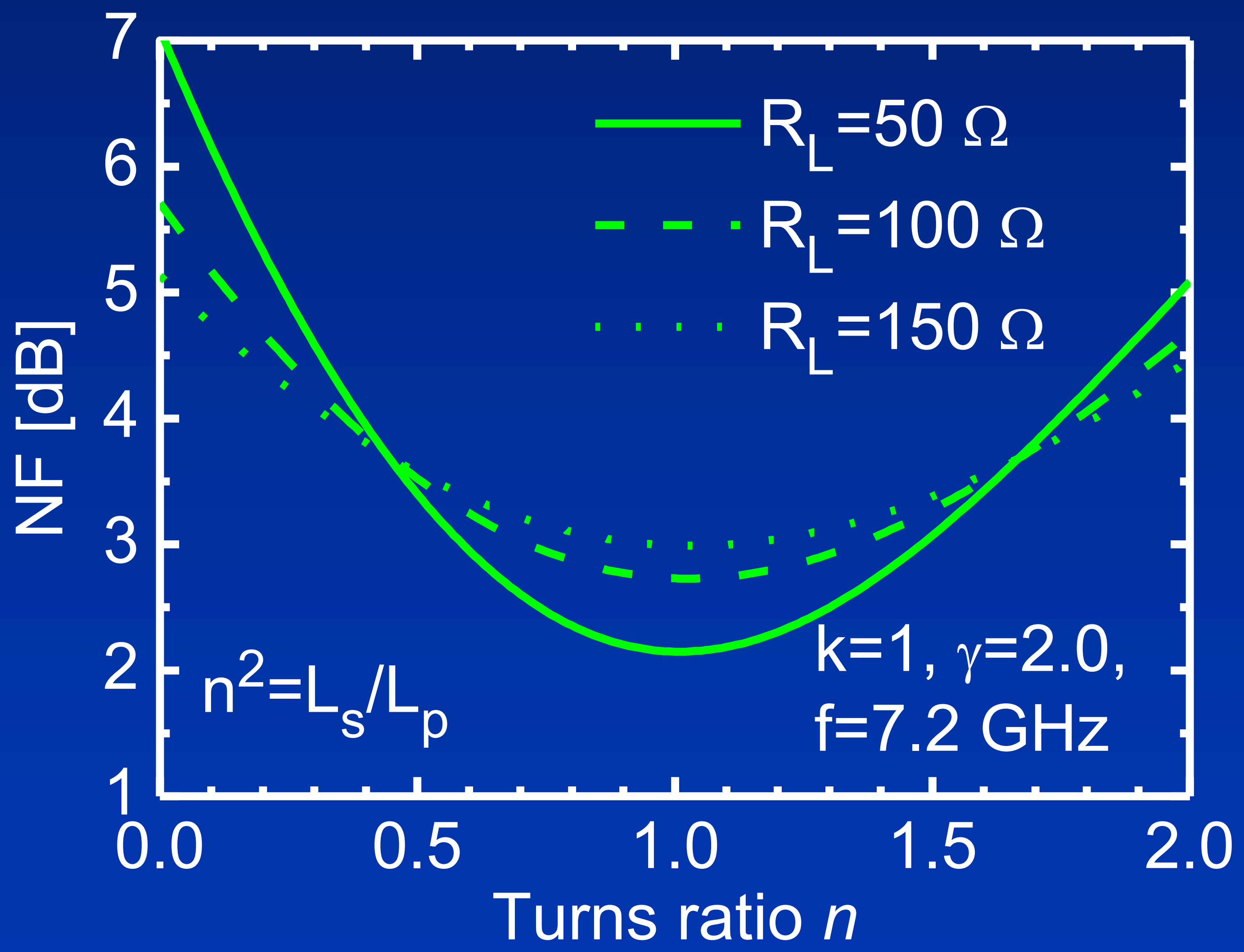
1. The noise current due to v_{nRL} flows from L_s into Z_L
2. The transformer induces v'_{nRL}
3. M_1 detects v'_{nRL}, and drains the noise current to the input

↓

The transformer reduces the effect of v_{nRL}

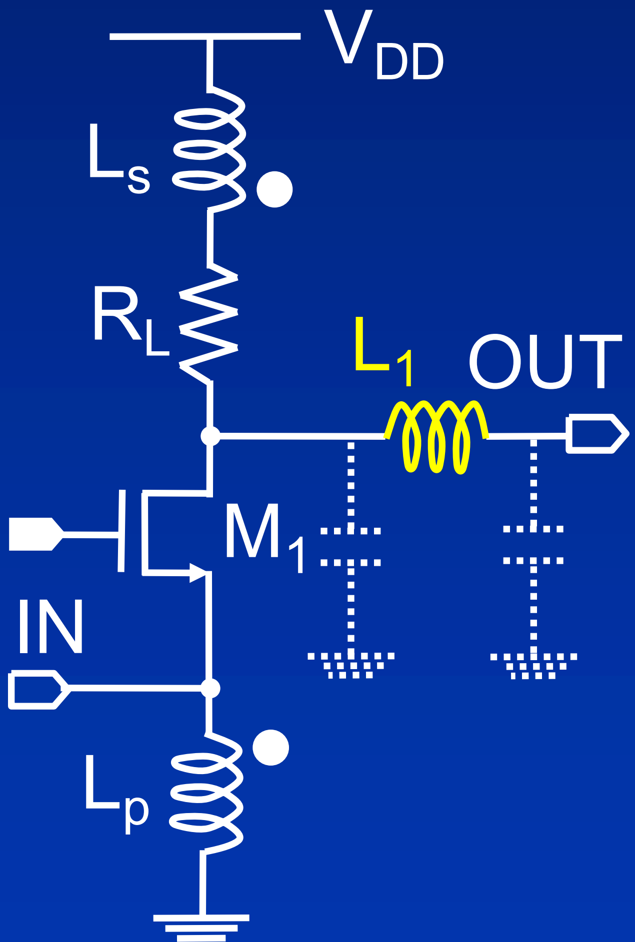


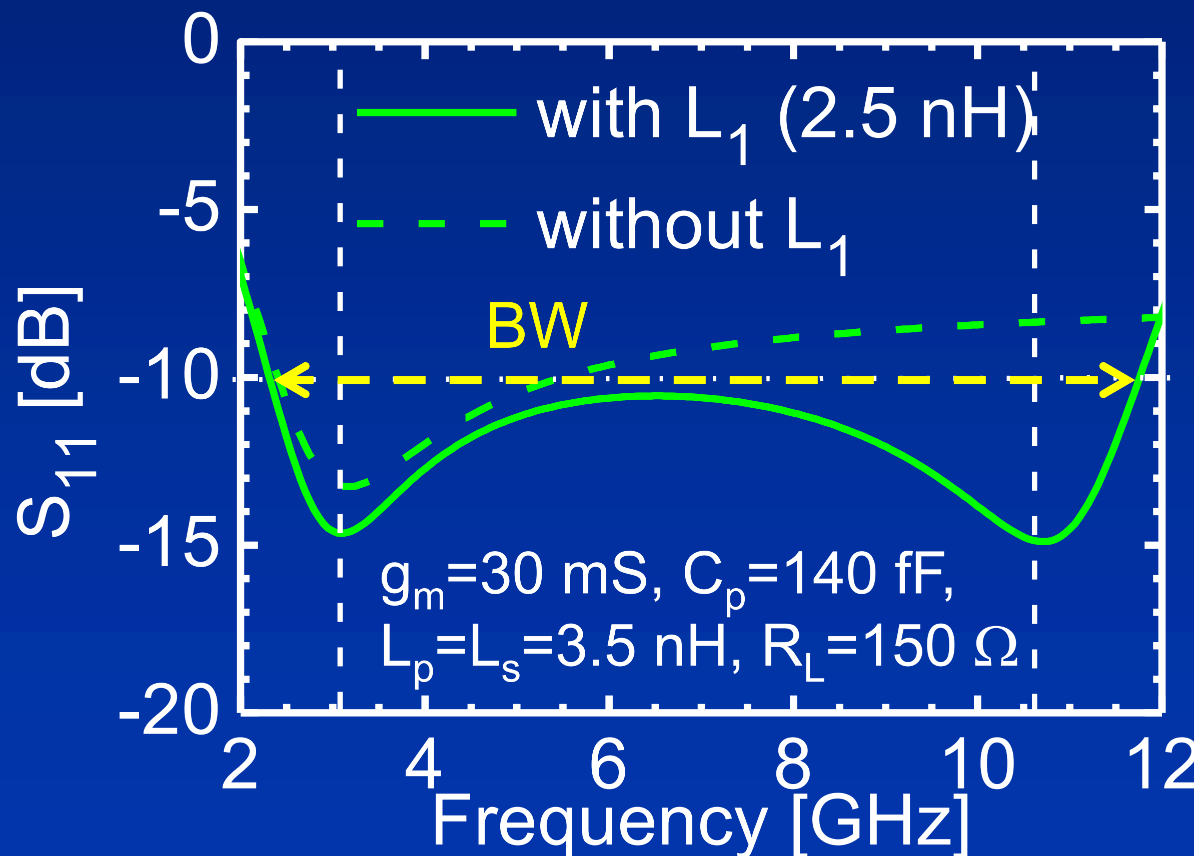
Optimization of Turns Ratio



n=1 provides the best noise performance

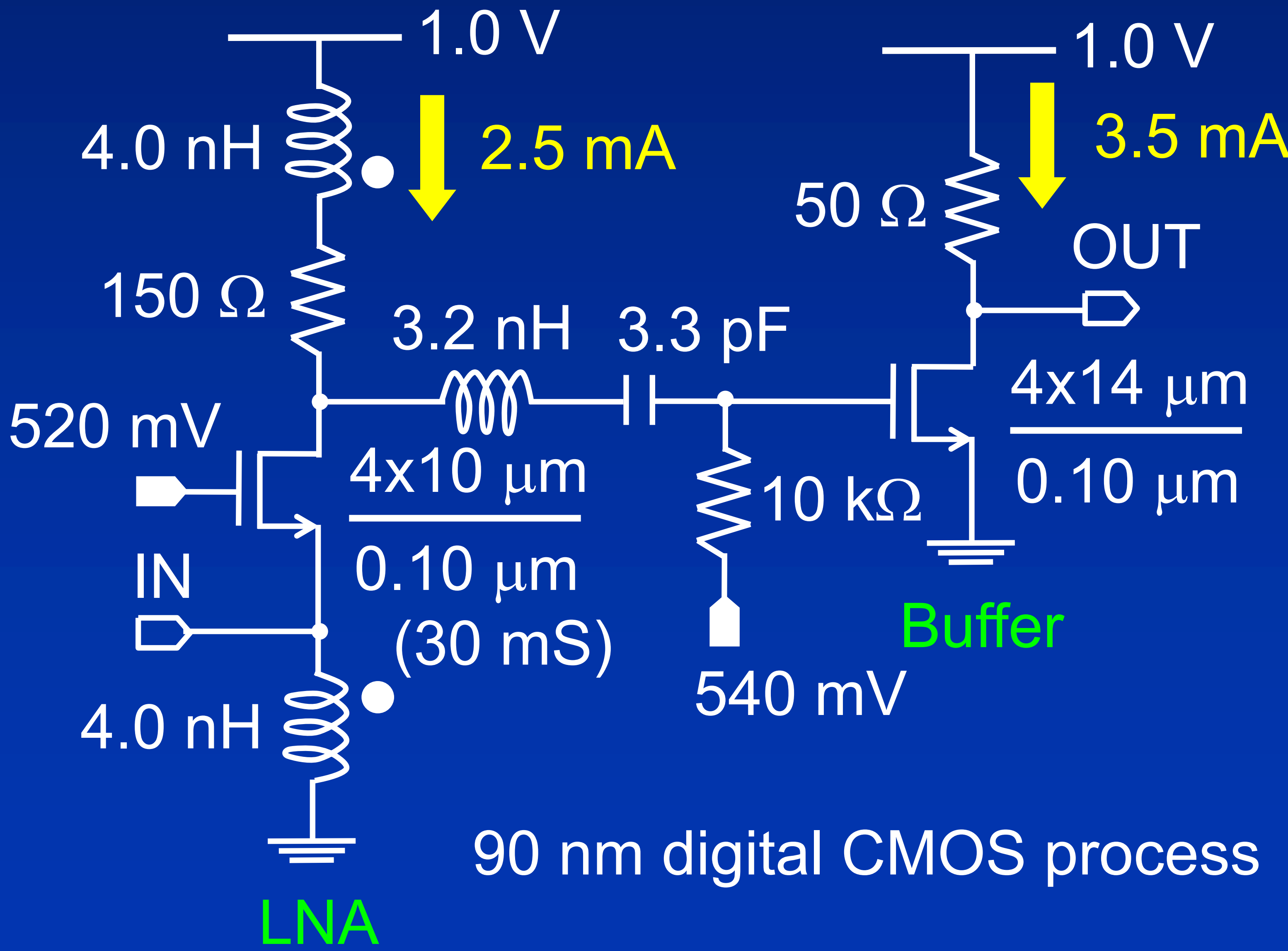
Wideband Impedance Matching





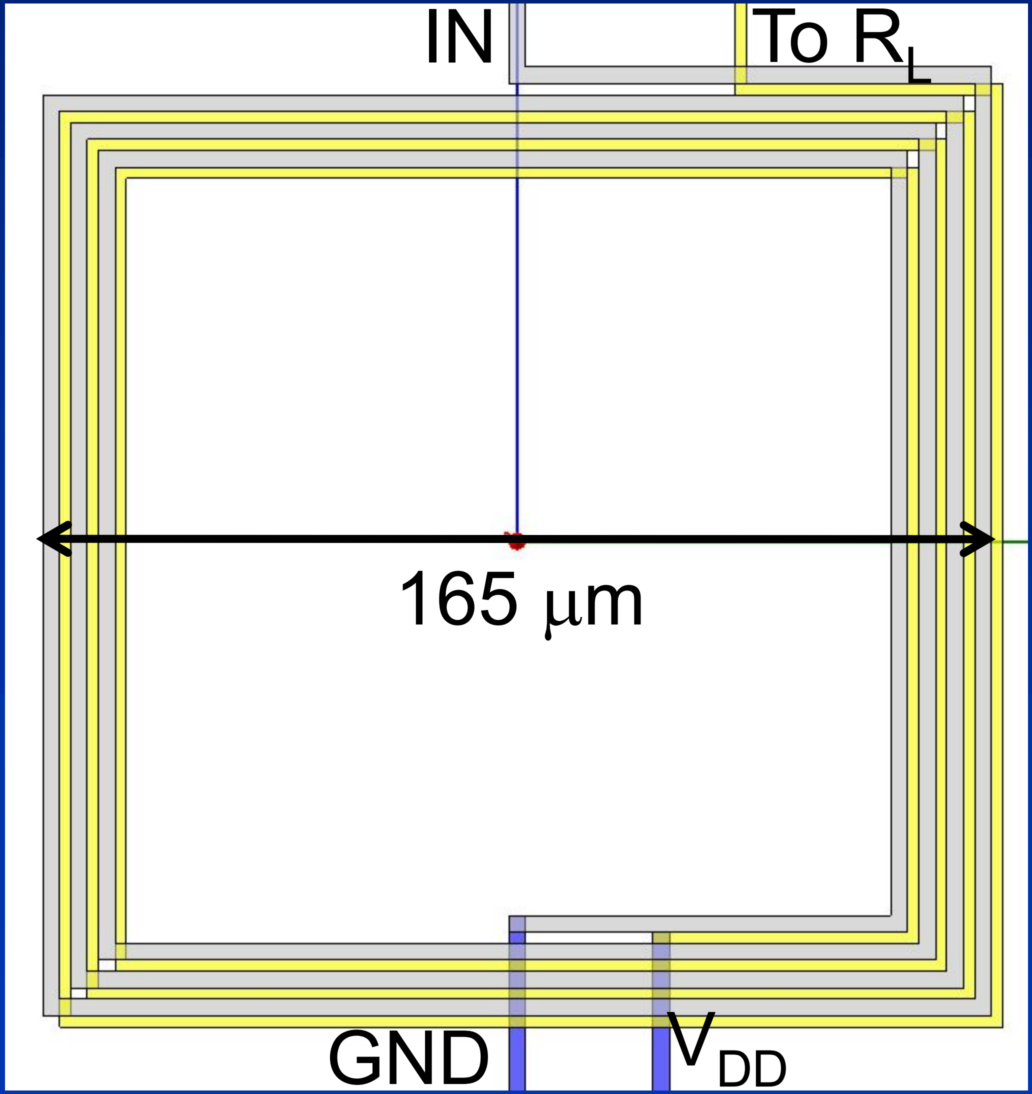
L_1 resonates with output parasitic capacitors, and increases the input bandwidth

Schematic of Designed LNA



90 nm digital CMOS process

Layout of Transformer



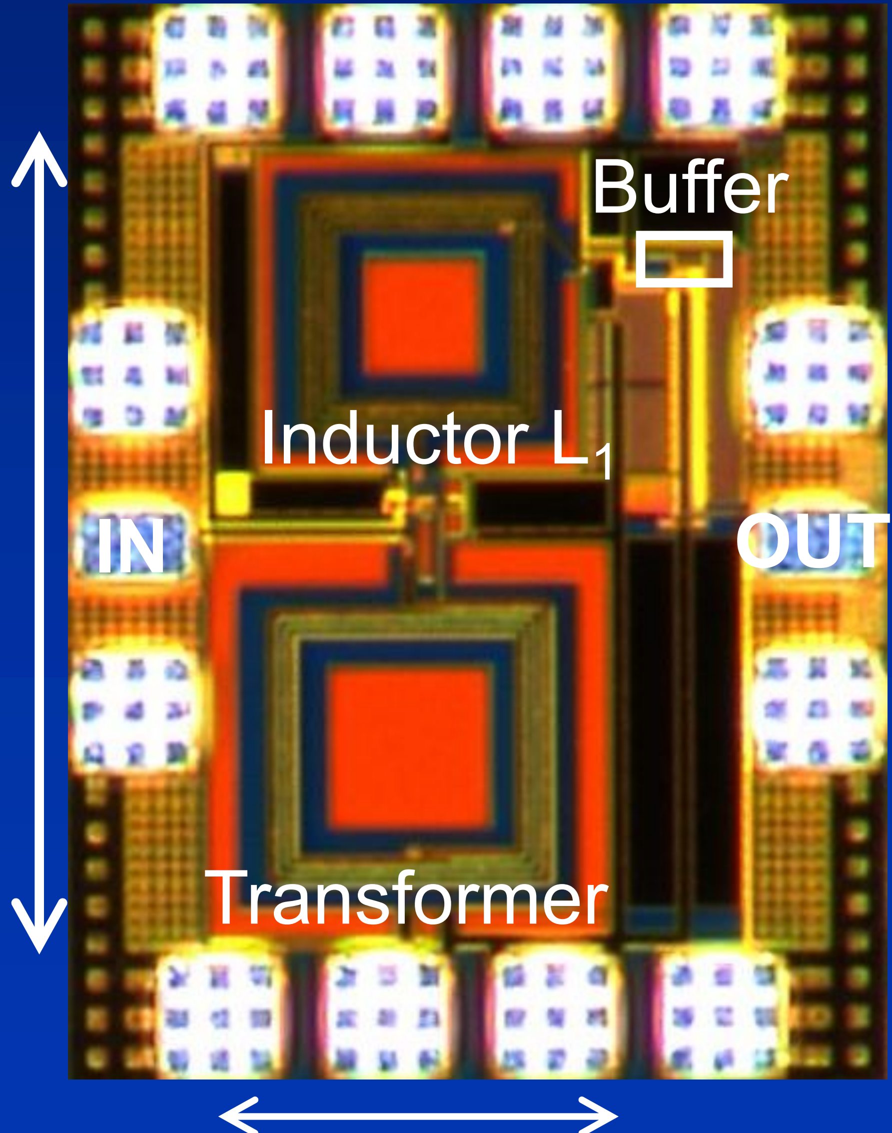
Primary inductor
(grey line, top pad metal)
Width: 3 μm
Spacing: 2 μm

Secondary inductor
(yellow line, metal 6)
Width: 2 μm
Spacing: 3 μm

From HFSS,
$L_p = L_s = 4.0$ nH, $k = 0.9$

A small chip area and large coupling factor

Microphotograph

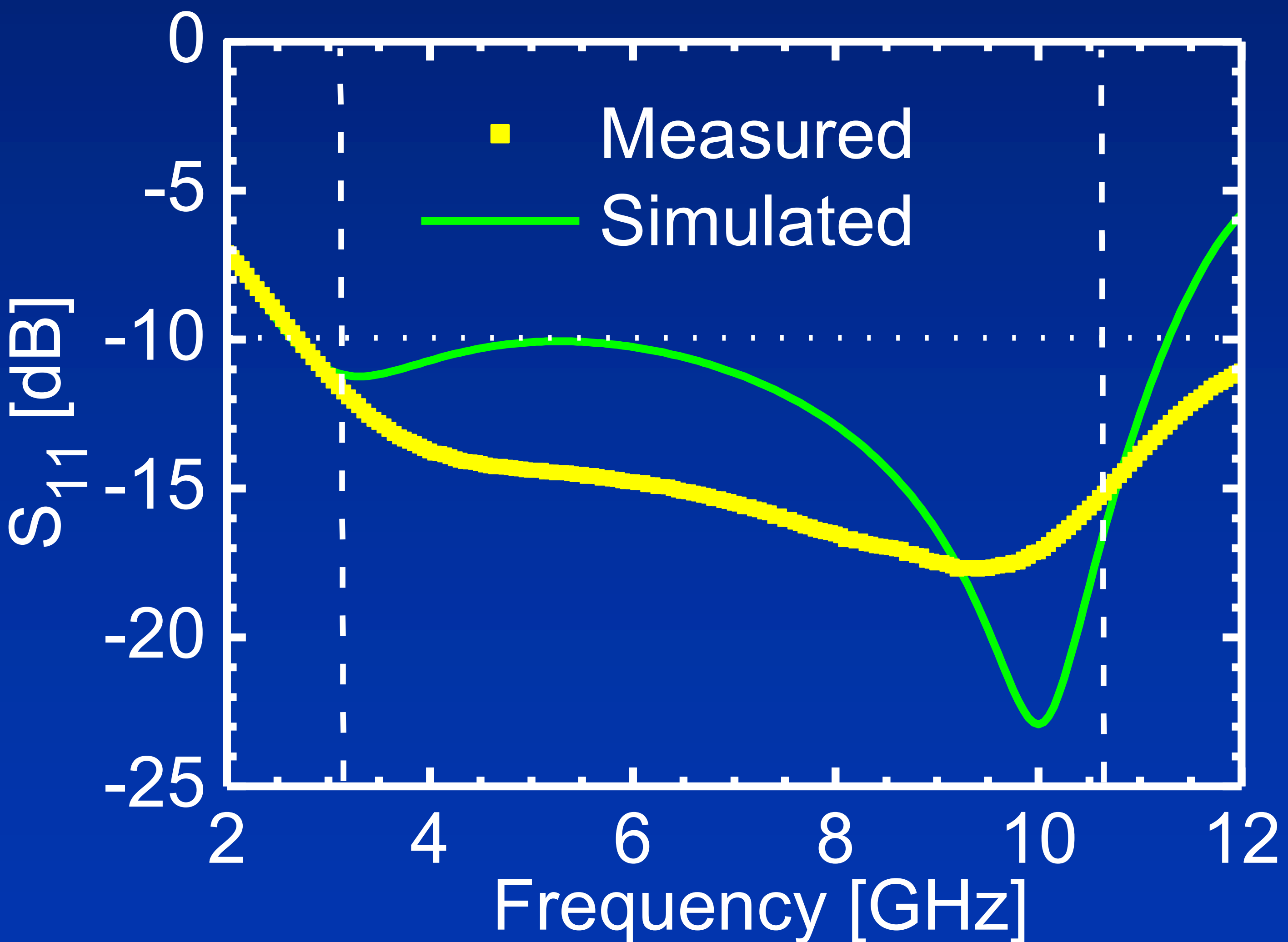


Technology:
90 nm 1P–6M digital CMOS

Chip area:
0.12 mm^2

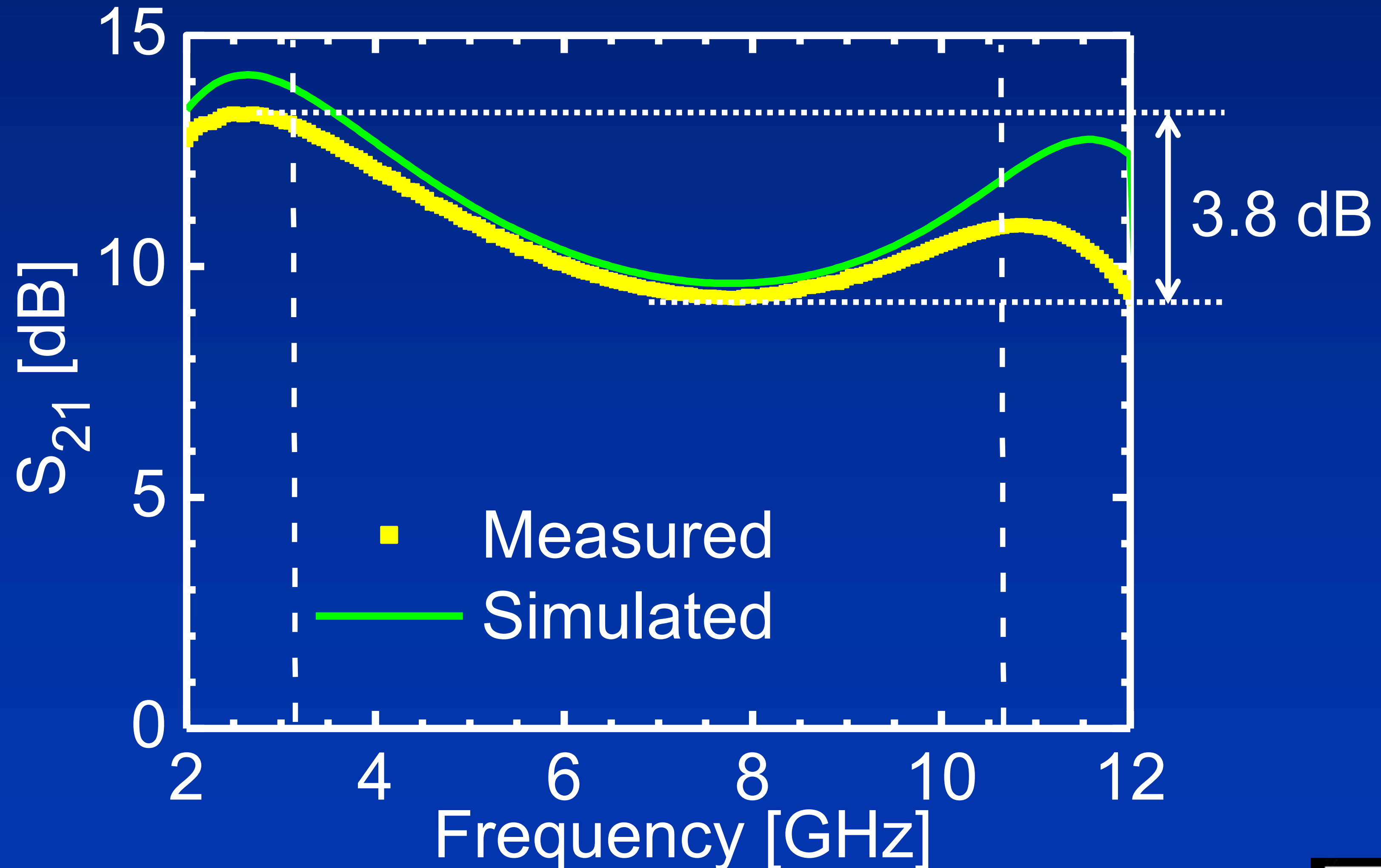
Input and output pads are not ESD protected

Measured and Simulated S_{11}



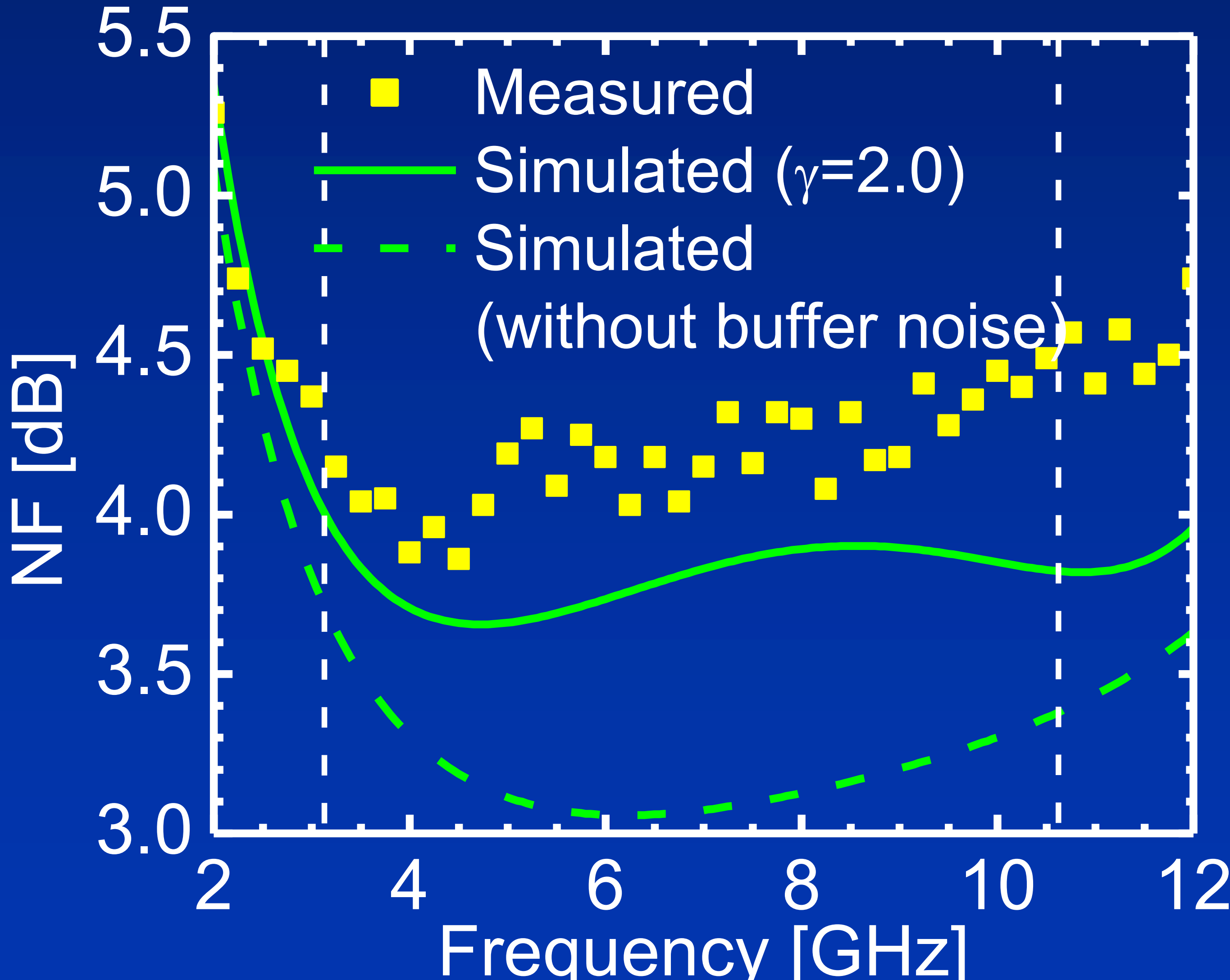
Measured S_{11}<-10 dB across 3.1–10.6 GHz

Measured and Simulated S_{21}



Measured S_{21}>9.3 dB across 3.1–10.6 GHz

Measured and Simulated NF



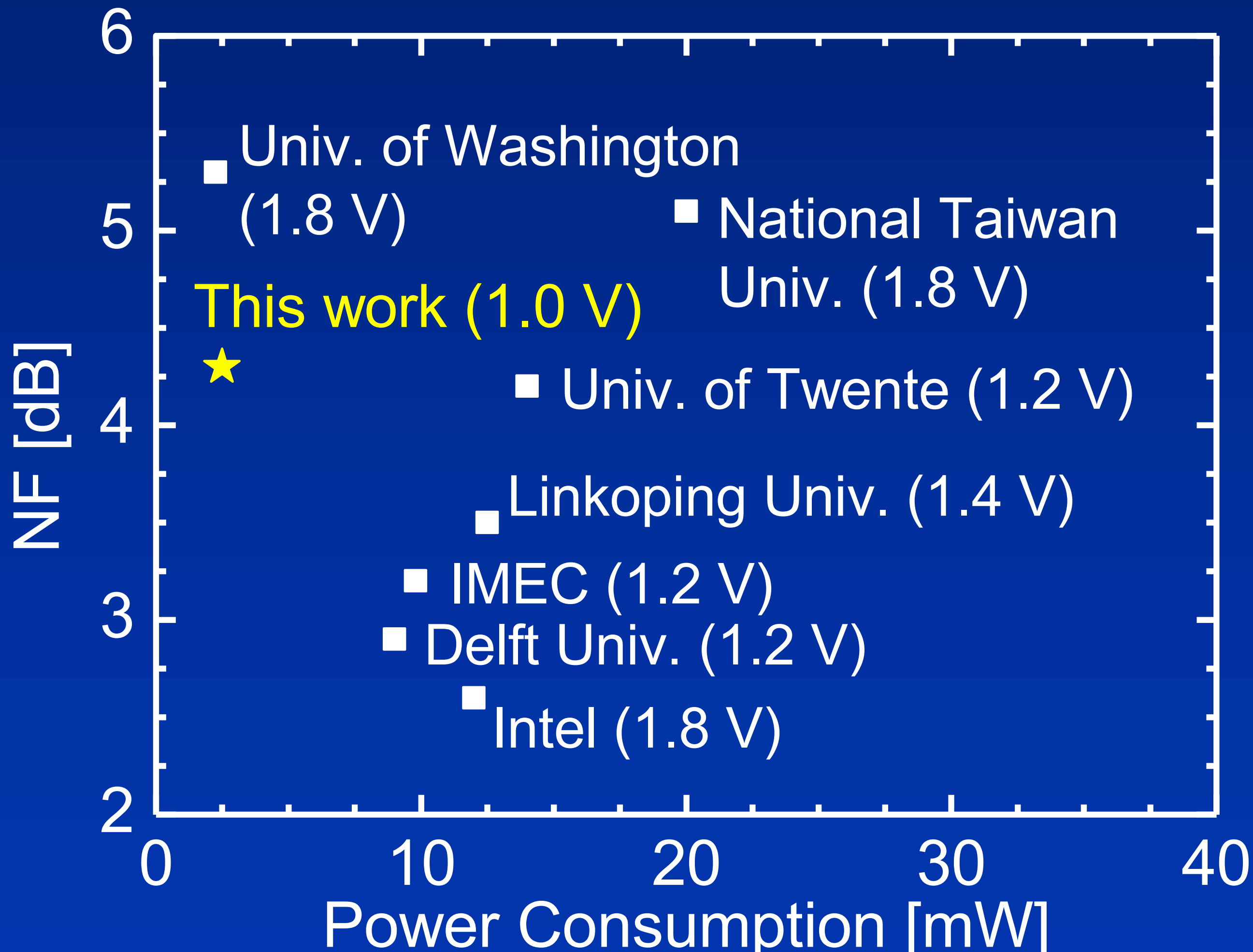
Measured NF<4.4 dB across 3.1–10.6 GHz

Performance Summary

	Process	BW* [GHz]	NF [dB]	S_{21} [dB]	IIP_3 [dBm]	Supply [V]	Power [mW]	Area [mm^2]
Spec.	N/A	3.1–10.6	<4.0	>10	N/A	N/A	N/A	N/A
This work	**90 nm CMOS**	**2.8–13.2**	**3.8–4.4**	**>9.3**	**>-9.3**	**1.0**	**2.5**	**0.12**

* BW is defined as the input bandwidth

Noise Figure Comparison



This LNA achieves a comparable NF with the lowest power consumption and supply voltage

Summary

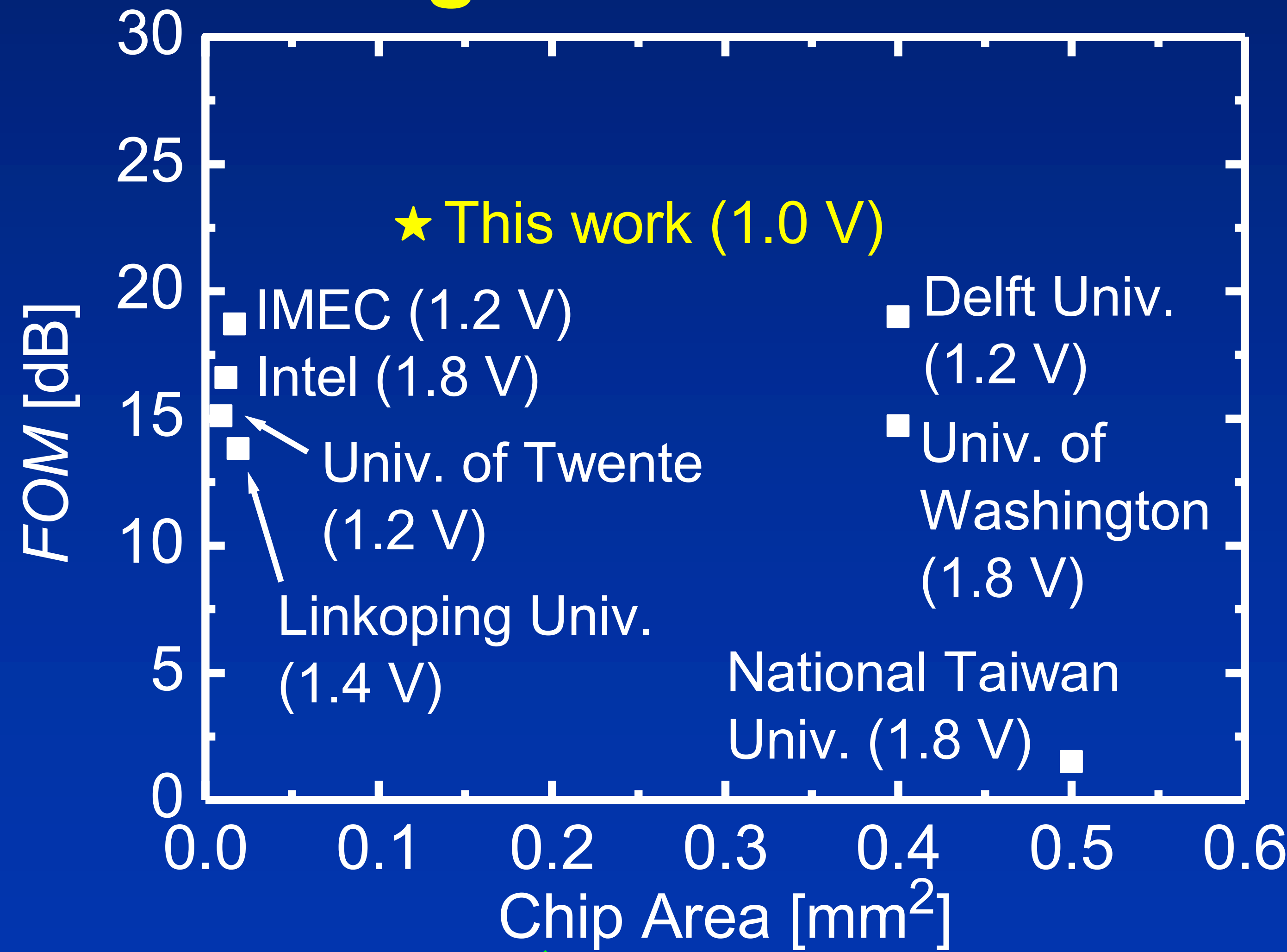
- The transformer partly cancels the noise of the common-gate transistor and load resistor
- The output series inductor increases the input bandwidth
- S_{11}<-10 dB, S_{21}>9.3 dB, NF<4.4 dB across 3.1–10.6 GHz with 2.5 mW from 1.0 V supply

The proposed LNA is the most suitable for low-power and low-voltage UWB CMOS LNAs

Acknowledgment

- VLSI Design and Education Center (VDEC)
- STARC
- Fujitsu Limited.
- Matsushita Electric Industrial Company Limited.
- NEC Electronics Corporation
- Renesas Technology Corporation
- Toshiba Corporation
- JSPS Global COE Program
- JSPS Initiatives

Figure of Merit



$$FOM\ [\text{dB}] = 20\log_{10}\left(\frac{Gain\ [\text{lin}] \times BW\ [\text{GHz}]}{Power\ [\text{mW}] \times (NF\ [\text{lin}] - 1)}\right)$$

Noise Cancellation Mechanism (1)

1. i_{nd} flows through L_s and R_L, generating v_{n1}
2. i_{nd} also flows through L_p, producing v_{n2}
3. The transformer induces v'_{n2}

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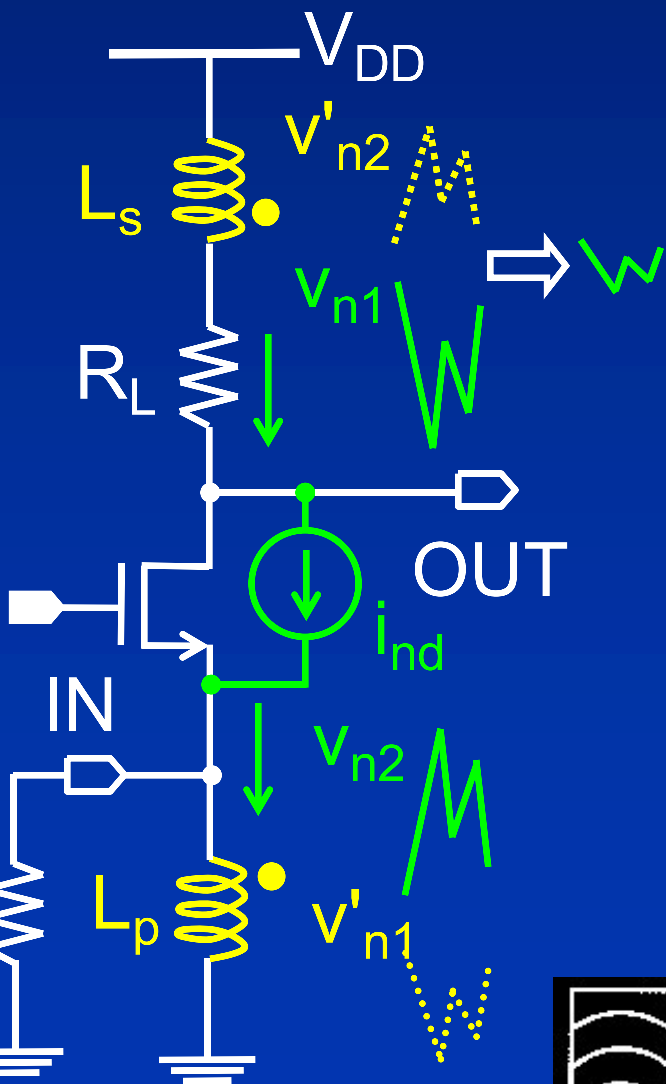
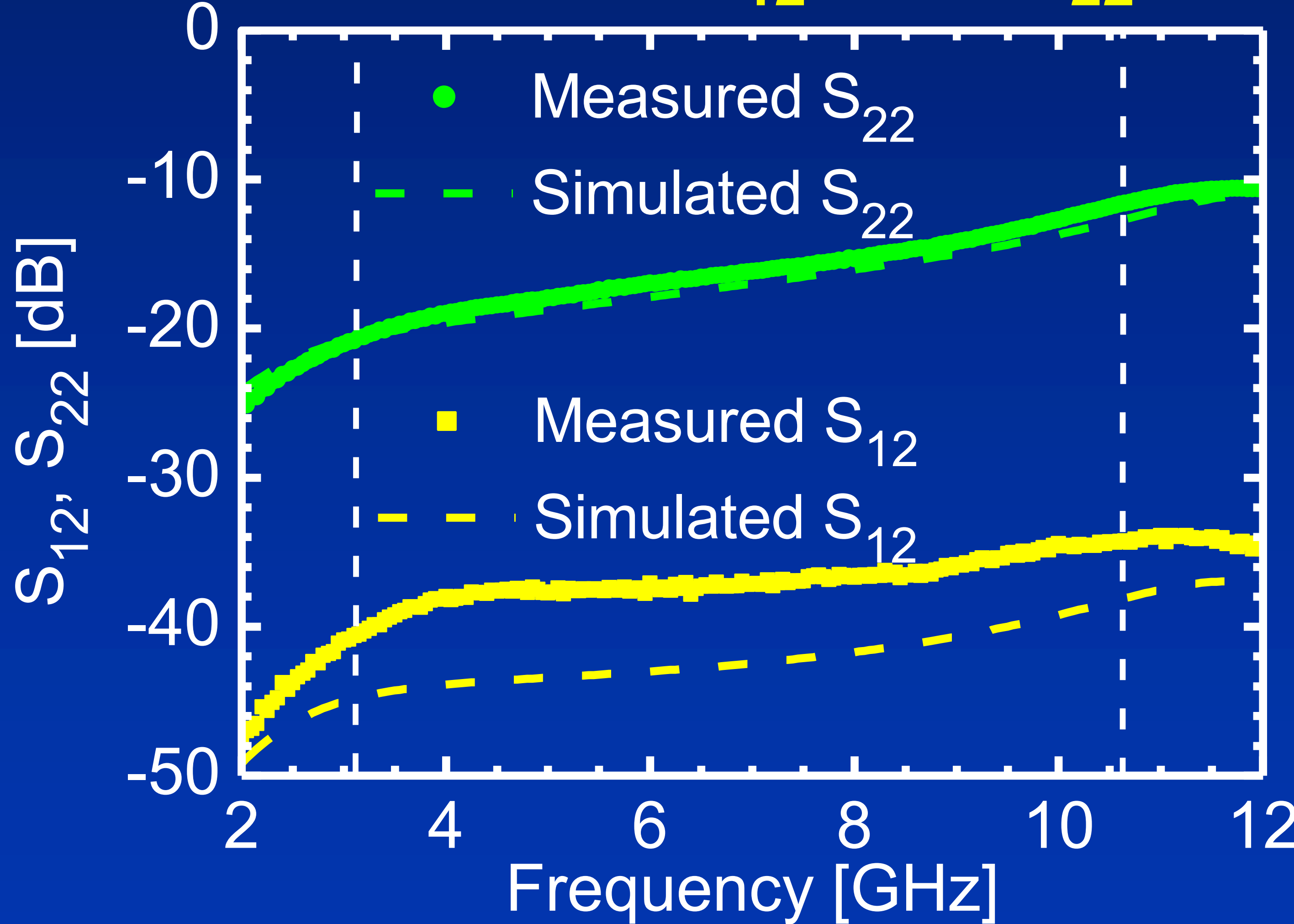
The transformer reduces the effect of i_{nd}

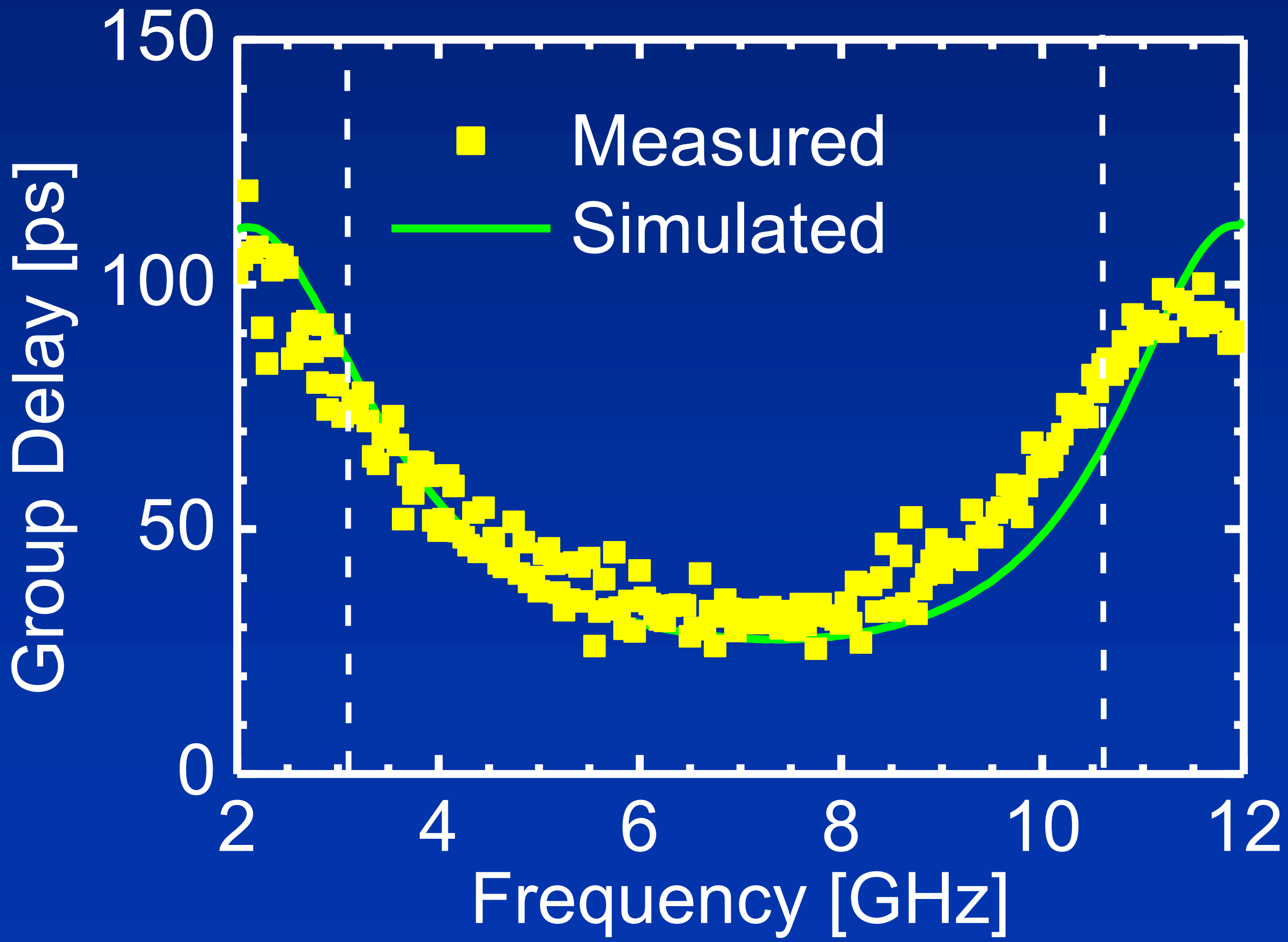


Measured S_{12} and S_{22}



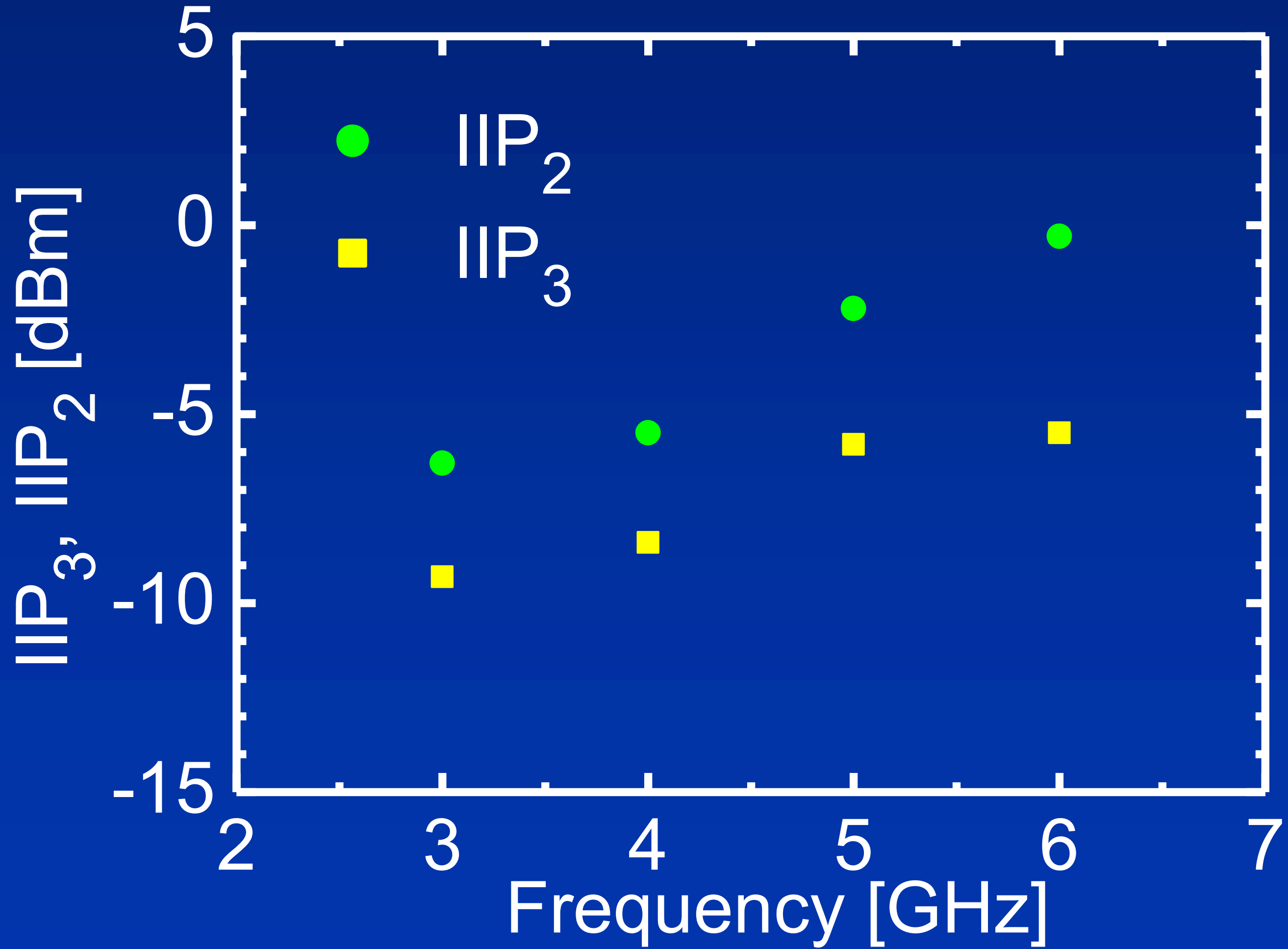
Measured S_{12}<-34 dB and S_{22}<-10 dB across 3.1–10.6 GHz

Measured Group Delay



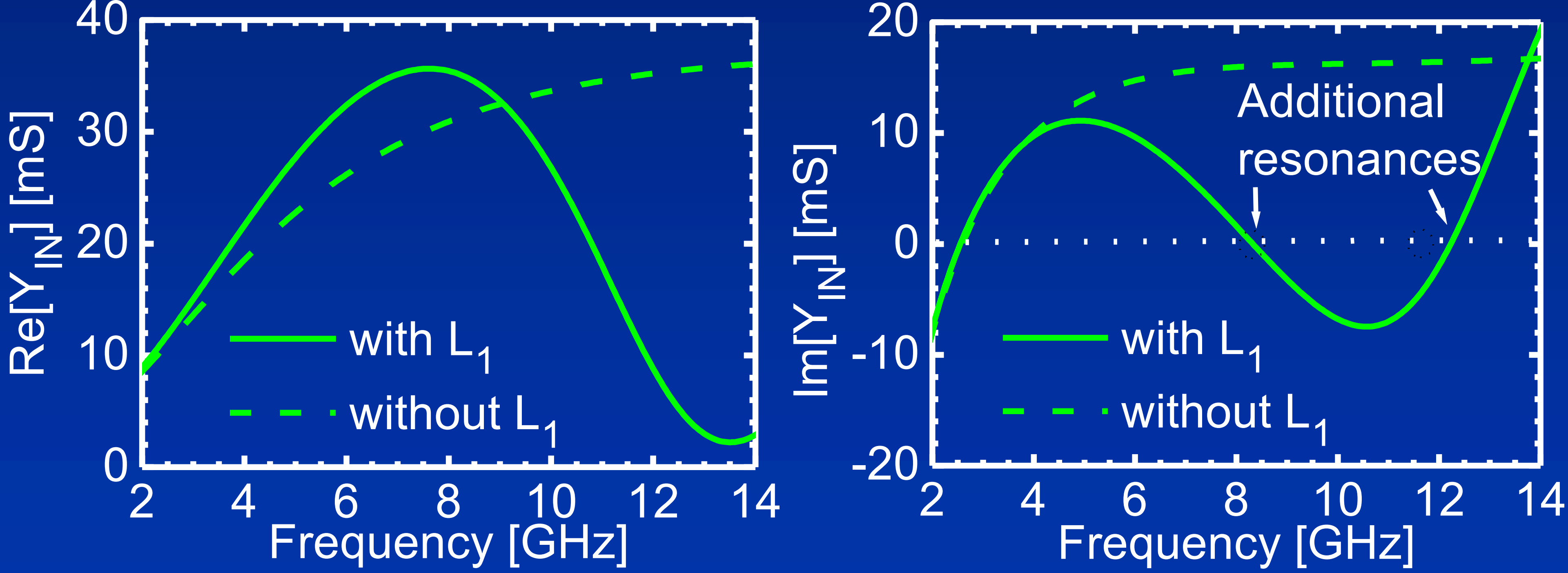
Measured group delay variation: 60 ps

Measured IIP_3 and IIP_2



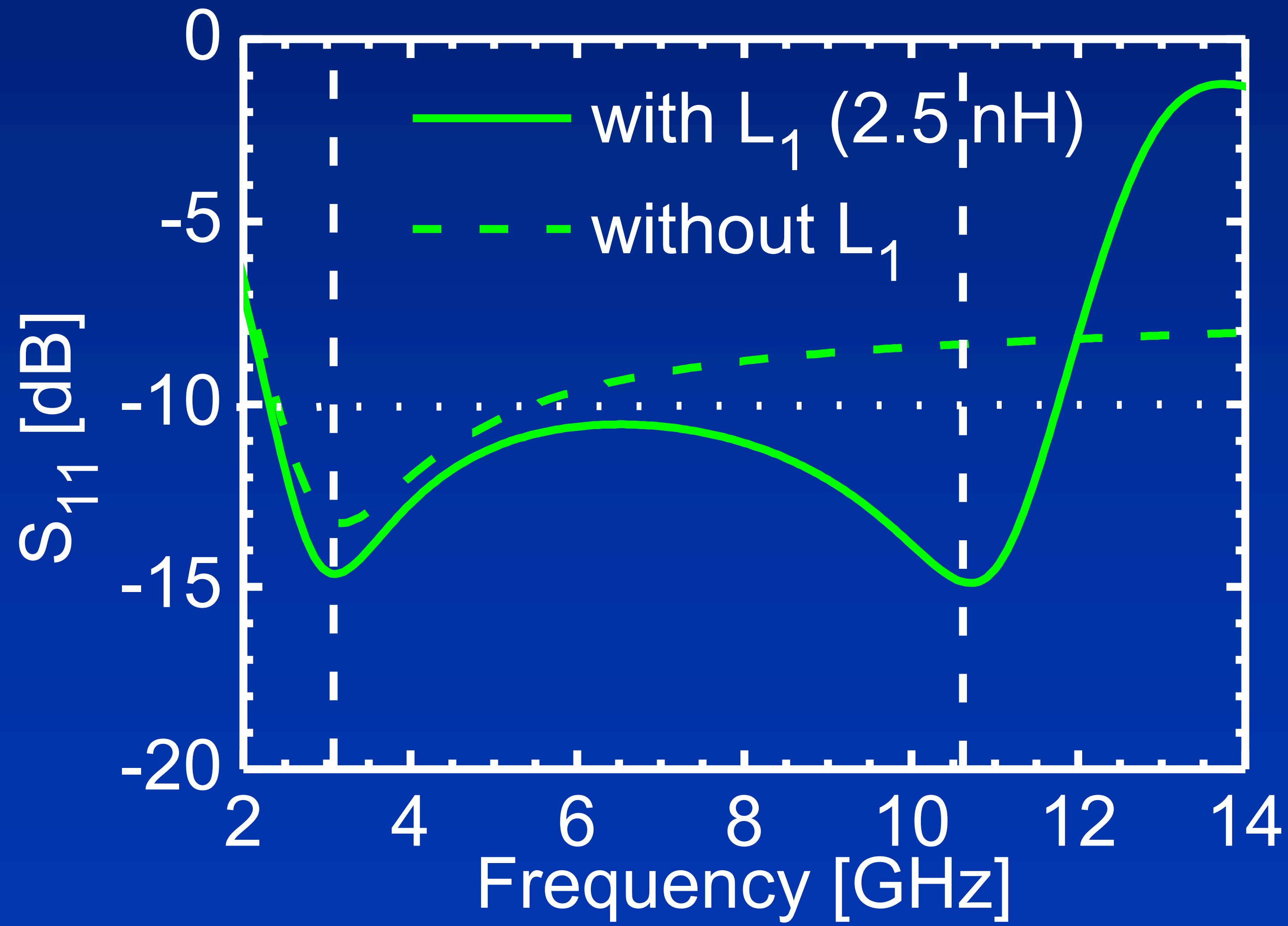
Measured IIP_3>-9.3 dBm and IIP_2>-6.3 dBm across 3.0–6.0 GHz

Calculated Input Admittance

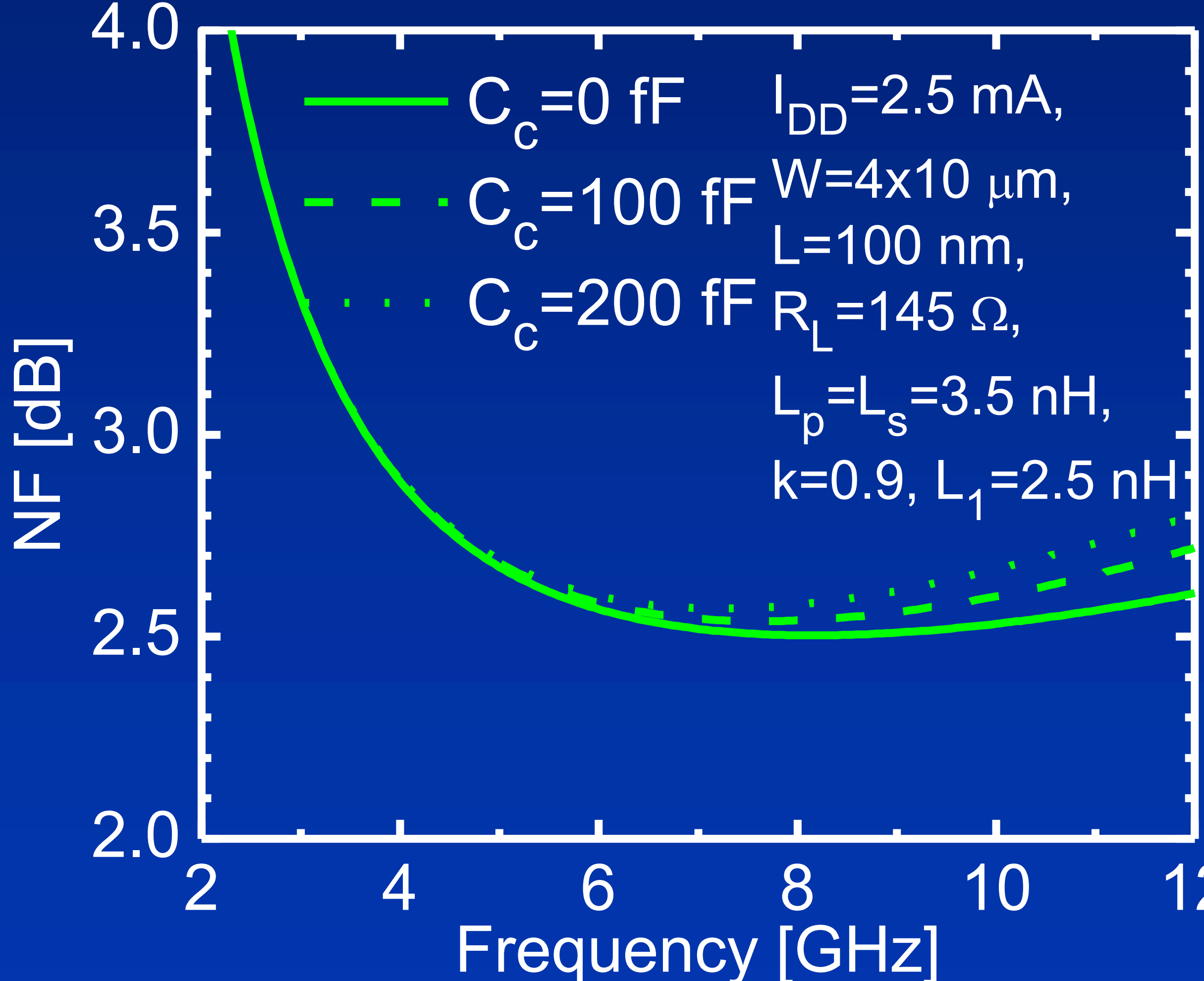


L_1 provides additional resonances at high frequencies

Calculated S_{11}

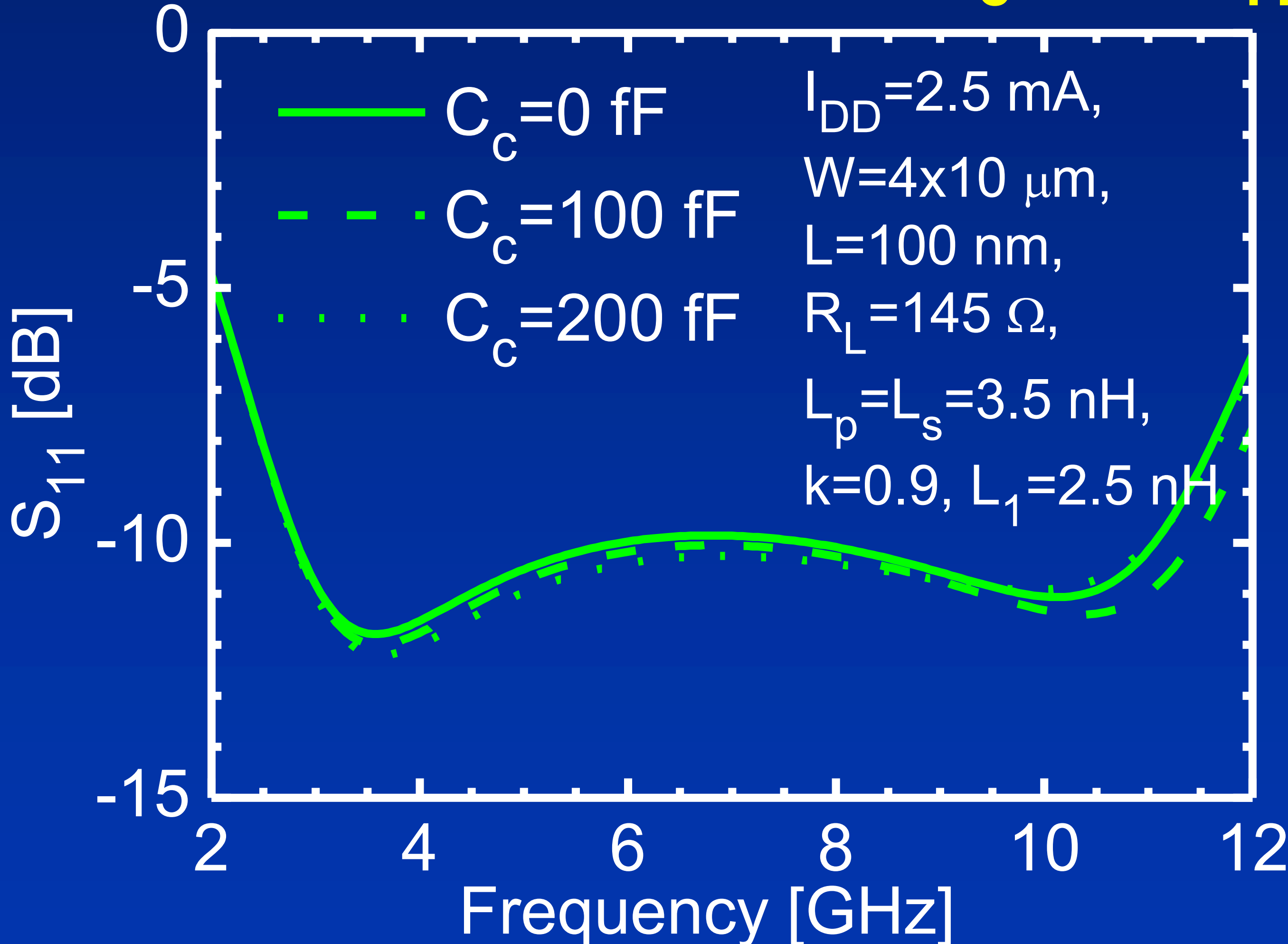


Simulated Effect of C_c on NF



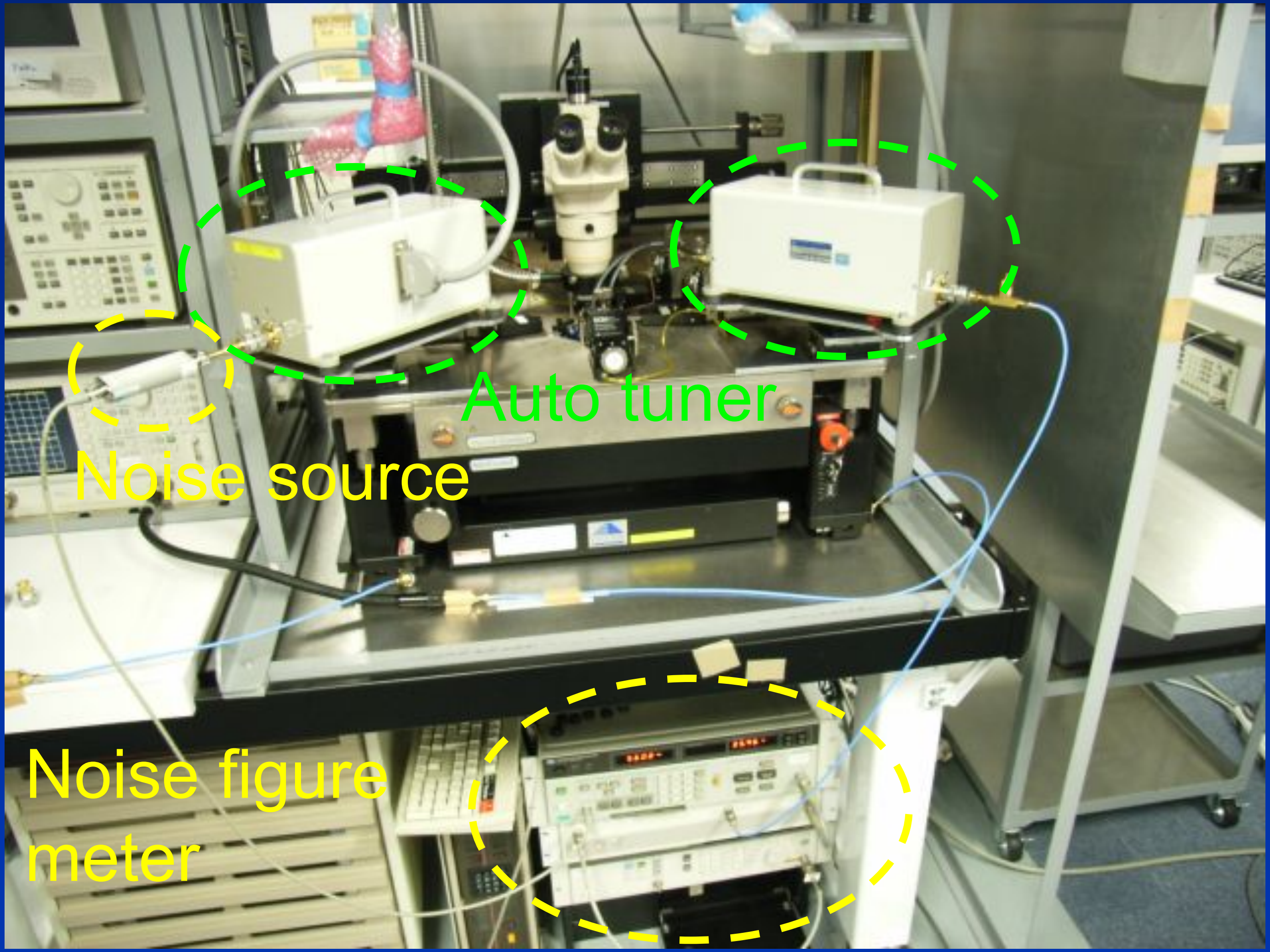
The parasitic capacitance between L_p and L_s increases NF by 0.2 dB

Simulated Effect of C_c on S_{11}



The parasitic capacitance between L_p and L_s has a small effect on S_{11}

Noise Figure Measurement



Probe Station