Digital Background Correction for Channel Mismatch and Third-Order Nonlinearity of TI-ADCs with VCOs

Takao Kihara
Osaka Institute of Technology, Japan

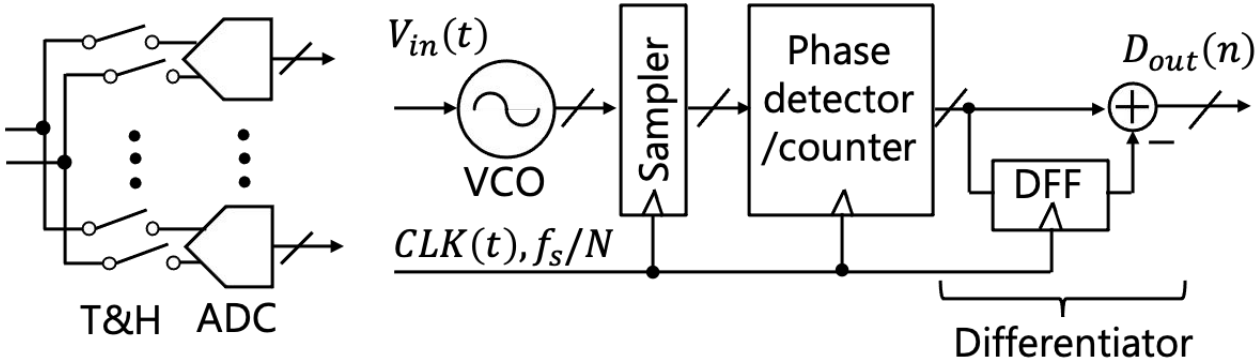
November 22-26, 2021

Outline

- Background and Objectives
  - Time-interleaved A/D converters (TI-ADCs) with voltage-controlled oscillators (VCOs)
  - Digital correction methods for TI-ADCs
- Correction Method
  - Expressions of mismatch aliasing and HD3 and IM3 products
  - Mismatch/HD3 and IM3 removals and estimations
- Simulations
  - Input and output FFT spectra
  - Layout and power consumption
- Comparison and summary

- ❏ HD3: Third-order harmonic distortion,
- ❏ IM3: Third-order Intermodulation
- ❏ FFT: Fast Fourier transform

TI-ADC with VCOs

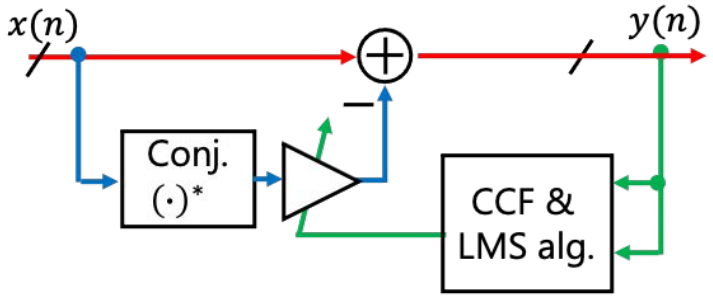


❑ SFDR: spurious-free dynamic range

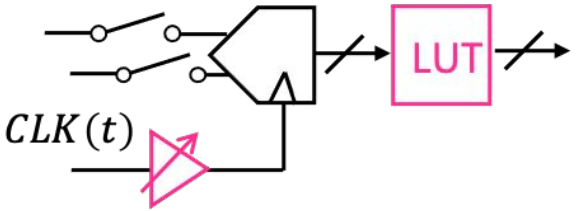
- Consists of multiple, N, VCO-based ADCs
- Reduces quantization noise around $+/-kfs/N$ (k=1, 2, …), i.e., bandpass
- Achieves 5 GS/s with 7.2 bit and 22.7 mW (JSSC ‘20 [3])
- Realizes low-power direct-RF sampling receivers
- Suffers from mismatch aliasing signals and HD3/IM3 products caused by nonlinearity, degrading SFDR
- Needs background correction circuit

Digital Correction Methods for TI-ADCs

- Conventional methods have not simultaneously corrected the channel mismatch and nonlinearity in background.
- TCAS-I ‘15 [4] and ‘19 [5] (my work):
  - Uses adaptive filters with CCF
  - Reduces mismatch aliasing signals
  - Not decreases HD3 and IM3
- JSSC ‘20 [3]:
  - Employs LUTs and tunable clock delays
  - Calibrates the mismatch and nonlinearity
  - Require CW signals and manual steps



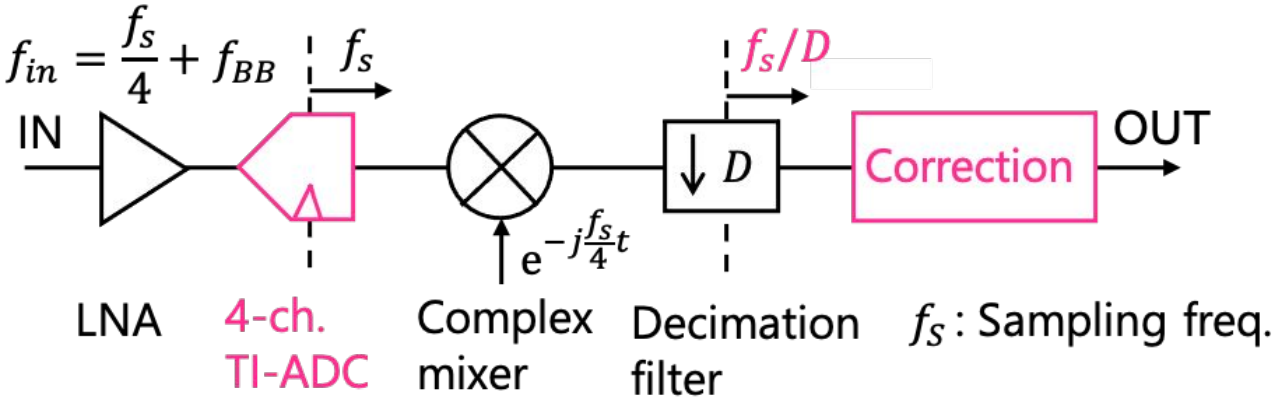
TCAS-I ’15 [4] and ’19 [5]



JSSC ’20 [3]

- CCF: Cross-correlation function,
- LUT: Lookup table,
- CW: Continuous wave

Objectives

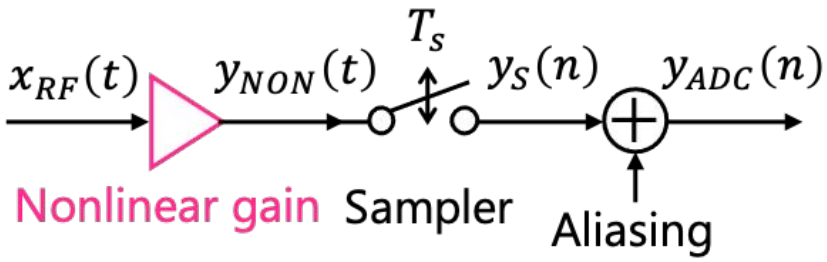


- ❏ LNA: Low-noise amplifier
- ❏ FP: Floating point

- Digital background correction for 4-ch. TI-ADC with VCOs:
  - Decreases mismatch aliasing signals, HD3, and IM3 products by using adaptive filters with CCF to improve SFDR from 54.8 dB to 66.7 dB
  - Utilizes bandpass (complex) signals, downconverted to DC and decimated by *D* in direct-RF receivers
  - Implemented by 24-bit FP arithmetic, operates at *fs/D* (=57.5 MS/s, where *fs*=3,680 MHz and *D*=64) and 4.3 mW for 65-nm CMOS process

Expressions of HD3 and IM3

- Bandpass TI-ADC with nonlinearity

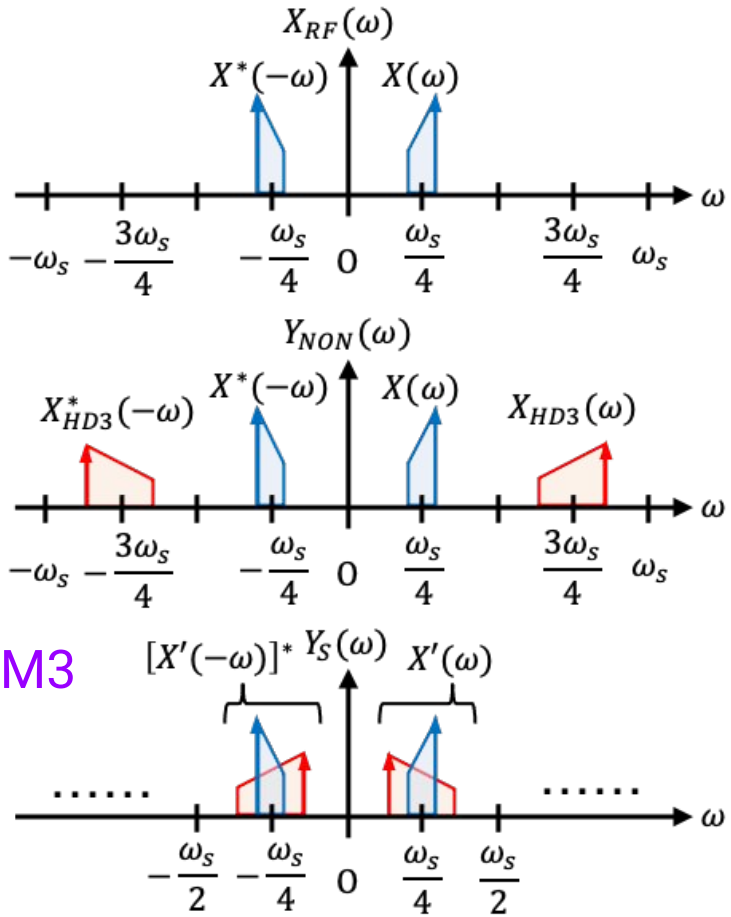


- $x_{RF}(t) = 2\,\mathrm{Re}[x(t)e^{j\frac{\omega_s}{4}t}] = x(t)e^{j\frac{\omega_s}{4}t} + x^*(t)e^{-j\frac{\omega_s}{4}t},$
- $y_{NON}(t) \approx a_1 x_{RF}(t) + a_2 x_{RF}^2(t) + a_3 x_{RF}^3(t),$

$$a_3 x_{RF}^3(t) = a_3\Big\{\underbrace{x^3(t)e^{j\frac{3\omega_s}{4}t} + [x^*(t)]^3 e^{-j\frac{3\omega_s}{4}t}}_{\text{HD3}} + \underbrace{3x^2(t)x^*(t)e^{j\frac{\omega_s}{4}t} + 3x(t)[x^*(t)]^2 e^{-j\frac{\omega_s}{4}t}}_{\text{IM3}}\Big\}$$

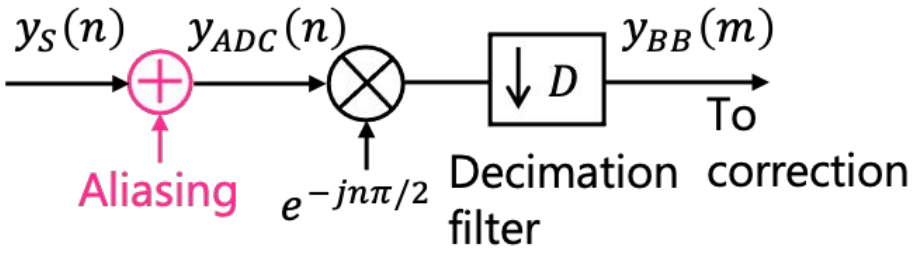
- $y_S(n) = y_{NON}(nT_s) = x'(n)e^{j\frac{\pi}{2}n} + [x'(n)]^* e^{-j\frac{\pi}{2}n},$

$$x'(n) = a_1 x(n) + a_3\Big\{\underbrace{[x^*(n)]^3}_{} + \underbrace{3x^2(n)x^*(n)}_{}\Big\},$$



Expression of Mismatch Aliasing

- TI-ADC with channel mismatch , followed by complex mixer and decimator.

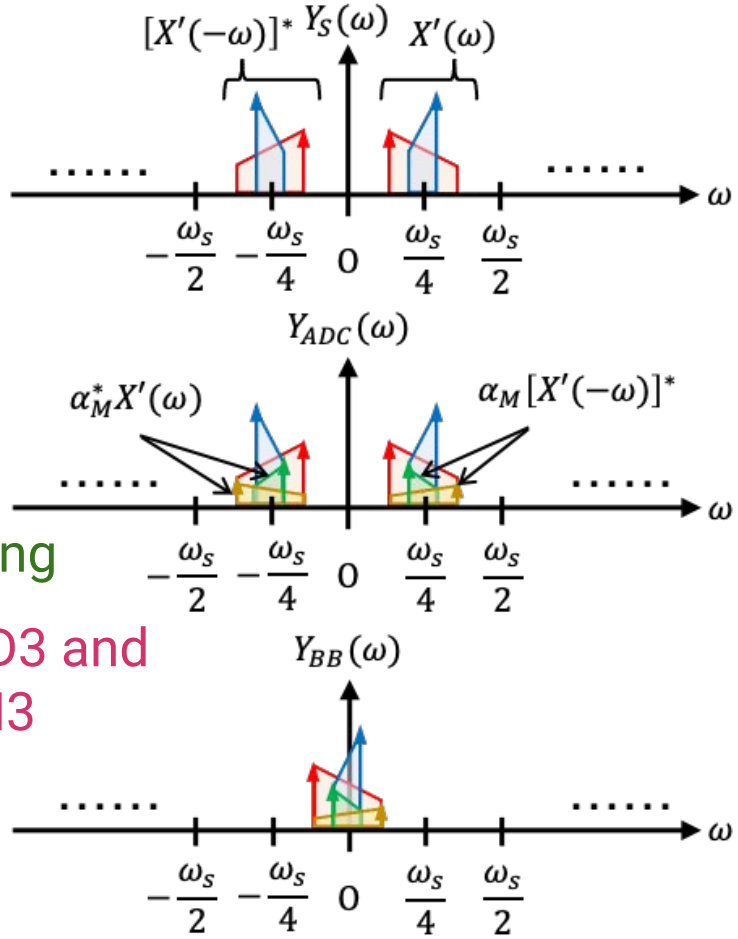


- $y_{ADC}(n) = y_{BB}(n)e^{j\frac{\pi}{2}n} + y_{BB}^*(n)e^{-j\frac{\pi}{2}n}$,

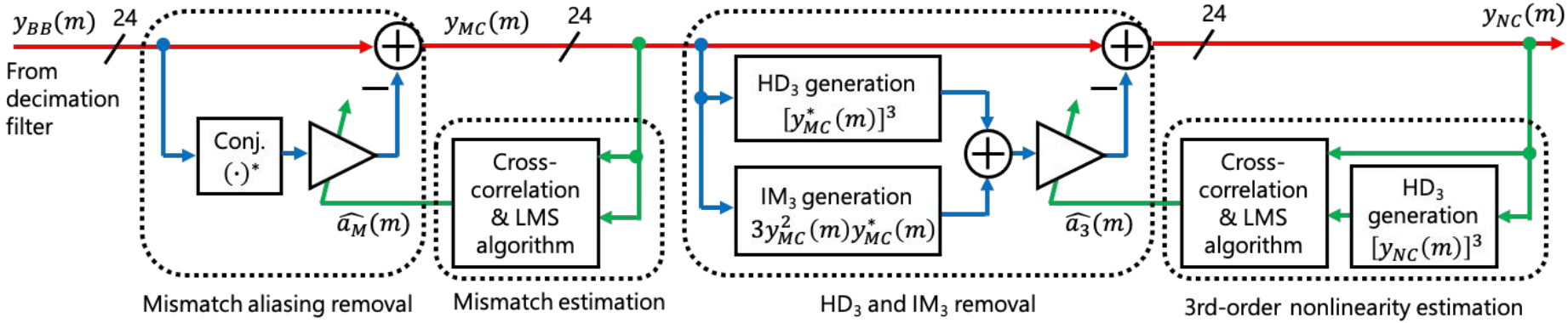
  $y_{BB}(n) = x'(n) + a_M^*[x'(n)]^*$, Mismatch aliasing

  $x'(n) = a_1 x(n) + a_3\{[x^*(n)]^3 + 3x^2(n)x^*(n)\}$, HD3 and IM3

If we estimate the coefficients exactly,
we can generate the same as these signals.



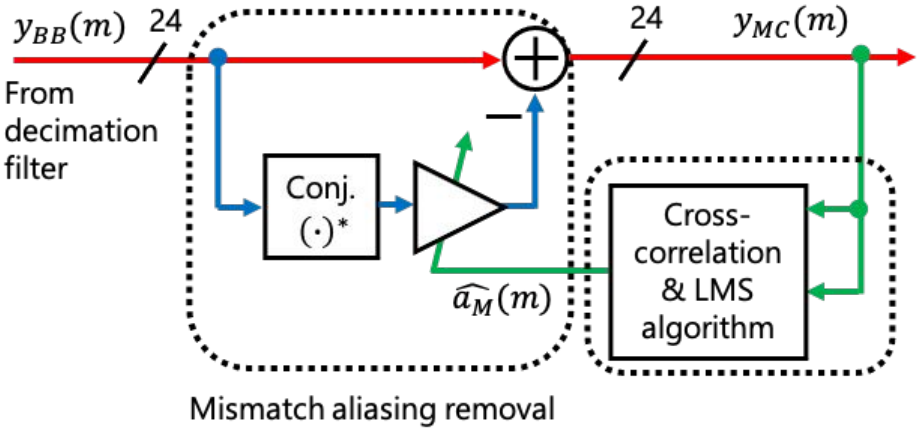
Correction Method

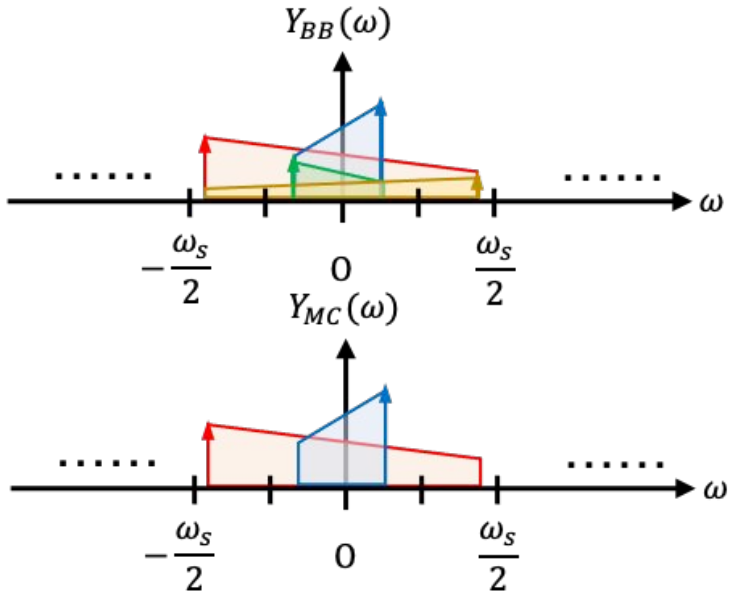


- Consists of four blocks: mismatch aliasing removal, mismatch estimation, HD3 and IM3 removal, and 3rd-order nonlinearity estimation
- Adaptive filters (removals) decrease mismatch aliasing signals/HD3 and IM3 products with $\widehat{a_M}(m)$/ $\widehat{a_3}(m)$, estimated by CCFs and LMS algorithms
- Implemented by 24-bit floating point arithmetic

❑ CCF: Cross-correlation function, LMS: Least mean square

Mismatch Removal and Estimation





- Removes mismatch aliasing:

$$y_{MC}(m) = y_{BB}(m) - \hat{a}_M(m-1)y^*_{BB}(m-1)$$

- Detects mismatch aliasing with CCF:

$$\gamma_{y_{MC}y^*_{MC}}(\tau) = E[y_{MC}(m)[y^*_{MC}(m-\tau)]^*] = E[y_{MC}(m)y_{MC}(m-\tau)],$$

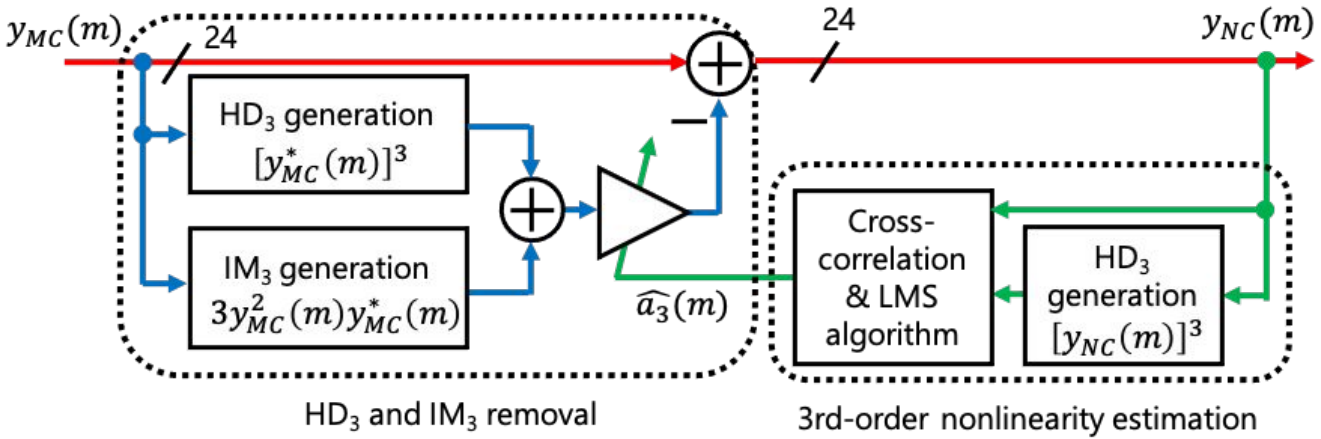
❑ $E[\cdot]$: Expected value

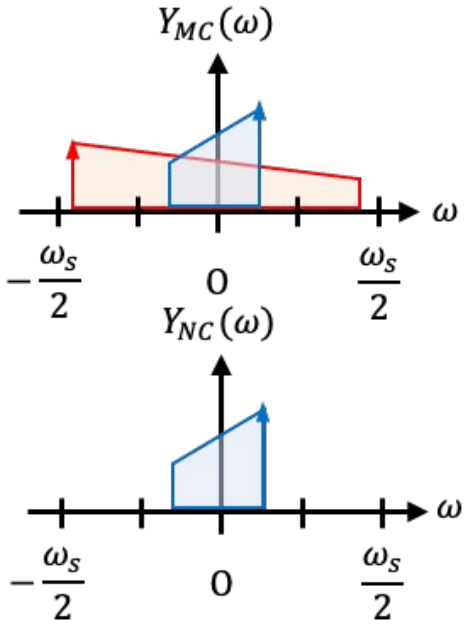
- LMS algorithm converges:

$$\hat{a}_M(m+1) = \hat{a}_M(m) + \mu_M \cdot \gamma_{y_{MC}y^*_{MC}}(\tau),$$

Adaptive step size

HD3 and IM3 Removals and HD3 Estimation





- Removes HD3 and IM3 products:

$$y_{NC}(m) = y_{MC}(m) - \hat{a}_3(m-1) \cdot \left\{ [y^*_{MC}(m)]^3 + 3y^2_{MC}(m)y^*_{MC}(m) \right\}$$

- Detects HD3 with CCF:

$$\gamma_{y_{NC}(y^*_{NC})^3}(\tau) = E[y_{NC}(m)y^3_{NC}(m-\tau)]$$

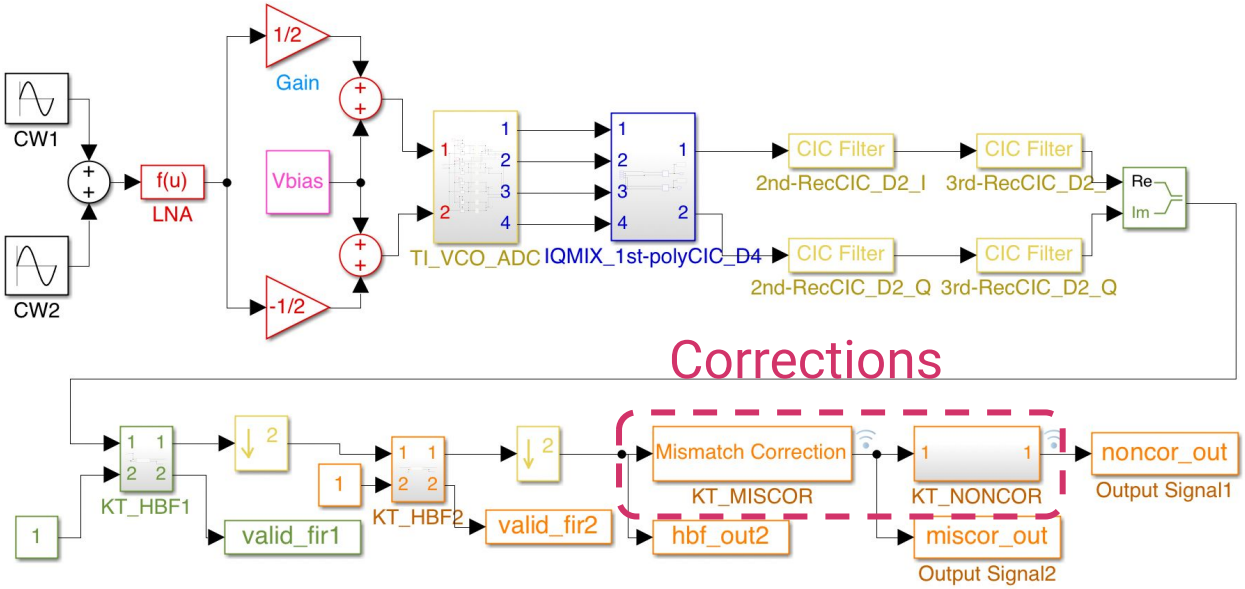
- LMS algorithm converges:

$$\hat{a}_3(m+1) = \hat{a}_3(m) + \mu_N \cdot \gamma_{y_{NC}(y^*_{NC})^3}(\tau),$$

Adaptive step size

Verification (Simulink Testbench)

- Proposed correction, applied to a direct-RF sampling receiver with fs=4x920 MHz, D=64, verified in:
  - System level: MATLAB/Simulink (Mathworks Inc.)



  - Circuit level: Analog/mixed-signal (AMS) simulator (Cadence Inc.)
    - Analog blocks (LNA, T&H circuits, VCOs, samplers, and clock generation circuits), designed with 65-nm CMOS PDK
    - Digital blocks including correction blocks, coded with Verilog-HDL

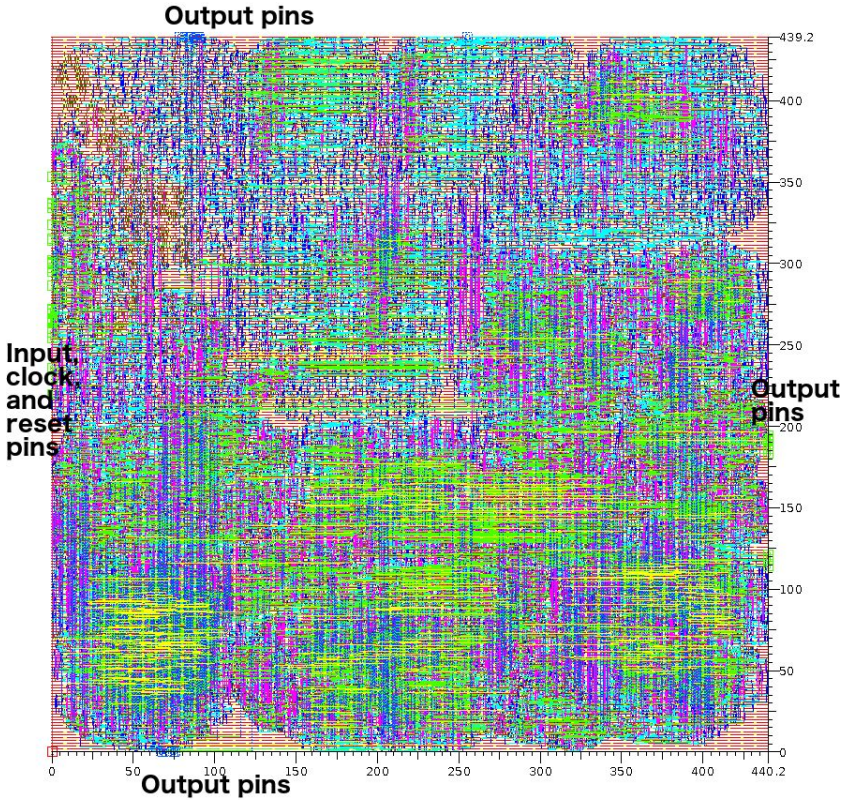
Simulated Conditions

Simulator	Parameter		Variable	Unit	Value
Common	Number of data		N_D	-	2^{21}
	Sampling frequency		f_s	MHz	4×920
	Frequencies of input two-tone signal		f_{in1}	MHz	924.04
			f_{in2}	MHz	925.84
	Power of input one-tone signal		P_{in1}, P_{in2}	dBm	-40.0
	Adaptive step size	Mismatch	μ_M	-	2^{-32}
		Nonlinearity	μ_N	-	2^{-72}
MATLAB/ Simulink	Gain of LNA		-	dB	20
	IIP_3 LNA		-	dBm	-0.50
	VCO gain coefficient	Bias	$a_{VCO,0}$	THz/V	0.088
		1st-order	$a_{VCO,1}$	THz/V	-0.669
		2nd-order	$a_{VCO,2}$	THz/V	1.995
		3rd-order	$a_{VCO,3}$	THz/V	-2.947
		4th-order	$a_{VCO,4}$	THz/V	-2.194
		5th-order	$a_{VCO,5}$	THz/V	-0.662

- Two-tone signal, around $fs/4$, input to receiver
- Nonlinearity coefficients of VCO, $a_{VCO,i}$ (i=1,2,3), for Simulink, obtained from circuits simulations

Layout and Power Comsuption of Digital Blocks

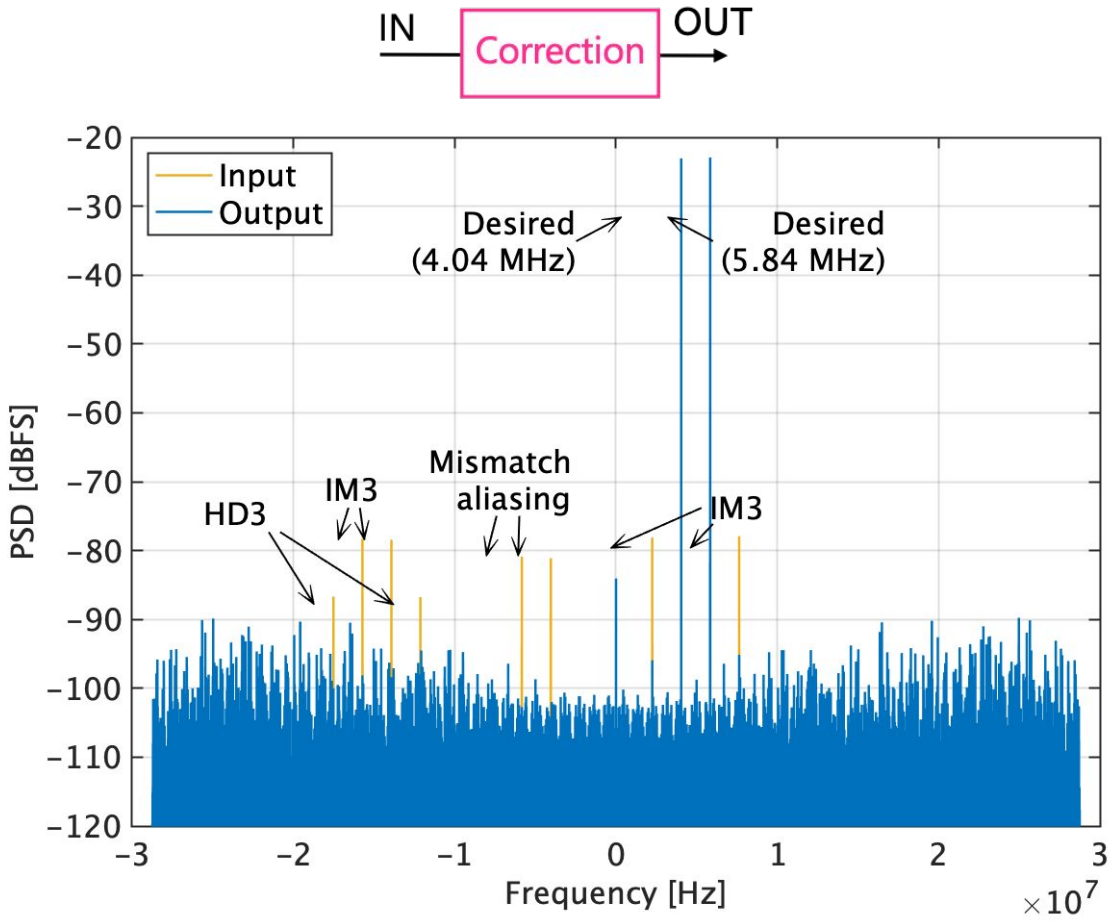
- Synthesized with Synopsys Design Compiler and 65-nm CMOS PDK
- Placed and routed with IC Compiler II for 920-MS/s (fs/N) rate and WST
- Chip area: 0.20 mm^2
- Dynamic and static power consumption of correction circuit: 4.3 mW (57.5-MS/s, fs/D) rate under TYP, set by a toggle rate of 60% on Synopsys Power Compiler



- WST cond. :SS, 0.9-V supply, and 125 deg.C
- TYP cond.: TT, 1.0-V supply, and 25 deg.C)

Simulated Input/Output FFT Spectra (Simulink)

- Desired signal (5.84 MHz) did not change
- Mismatch aliasing (−5.84 MHz) decreased from −80.8 dBFS to −102 dBFS
- HD3 (−17.52 MHz), reduced to −100 dBFS
- IM3 product (7.64 MHz), reduced to −95.1 dBFS
- Two-tone SFDR, improved from 54.8 dB to 66.7 dB



Comparison of Digital Corrections for TI-ADCs

	This work	M. Baert JSSC 2020 [4]	S. Singh TCAS-I 2015 [5]	Y. Qui TCAS-I 2018 [11]	G. Taylor JSSC 2013 [12]
Architecture	Adaptive filter	LUT, tunable delays	Adaptive filter	Adaptive filter	LUT, replica ADC
External signal	**No**	CW	No	No	No
Mismatch correction for TI-ADC	**Background**	Offline	Background	Background	No
Nonlinearity correction	**Background***	Offline	No	No	Background
Sampling freq. of (TI-)ADC, f_s [MHz]	3,680	5,000	2,900	32,000	1,300
Operating freq. [MHz]	**57.5** (f_s/D)	625 (f_s/N)	f_s	f_s	1,300 (f_s)
Power consumption [mW] @ Supply [V]	4.3@1.0	2.7@0.9	N/A	N/A	<8.5@0.9
Verification method/chip	Simulated/Custom	Measured/Custom	Simulated†/N/A	Measured/FPGA	Measured/Custom

* Only for third-order nonlinearity. † Measured TI-ADC data was used.

- Proposed method:
  - Simultaneously corrects the channel mismatches and third-order nonlinearity of TI-ADCs in the background
  - Operates at lower clock rates (fs/D) than the other correction circuits

Summary

- Digital background correction:
  - Reduces the mismatch aliasing signals, HD3, and IM3 products of four-channel TI-ADCs with VCOs.
  - Utilizes the complex and decimated data, sent from a direct-RF receiver, and adaptive filters with CCF of these signals.
  - Designed with 24-bit floating point arithmetic and a 65-nm CMOS technology
  - Improves the two-tone SFDR of a TI-ADC with fs=3,680 MHz from 54.8 dB to 66.7 dB, operating at 4.3 mW and a rate of 57.5 MS/s on simulations.