First-Order Recursive CIC Filters in Time-Interleaved VCO-Based ADCs for Direct-RF Sampling Receivers

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Outline

Background and objectives

- Direct-RF sampling receiver
- Conventional methods to lower power consumption

Proposed direct-RF sampling receiver

- Time-interleaved VCO-based ADC
- First-order recursive CIC filter

Simulations

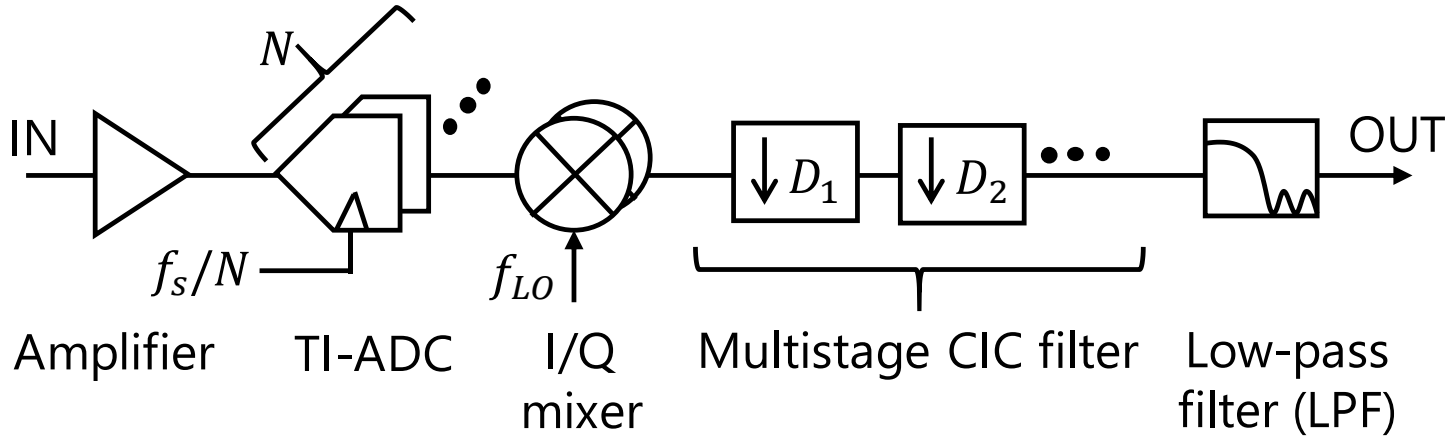
- Output spectrum (SNR)
- Chip area and power consumption
- Performance comparison

Summary

Background

Direct-RF sampling receivers:

- Consist of N-channel TI-ADCs, I/Q mixers, CIC filters, and LPFs
- Provide flexibility in designing RF receivers
- Reduce the design cost and time to market

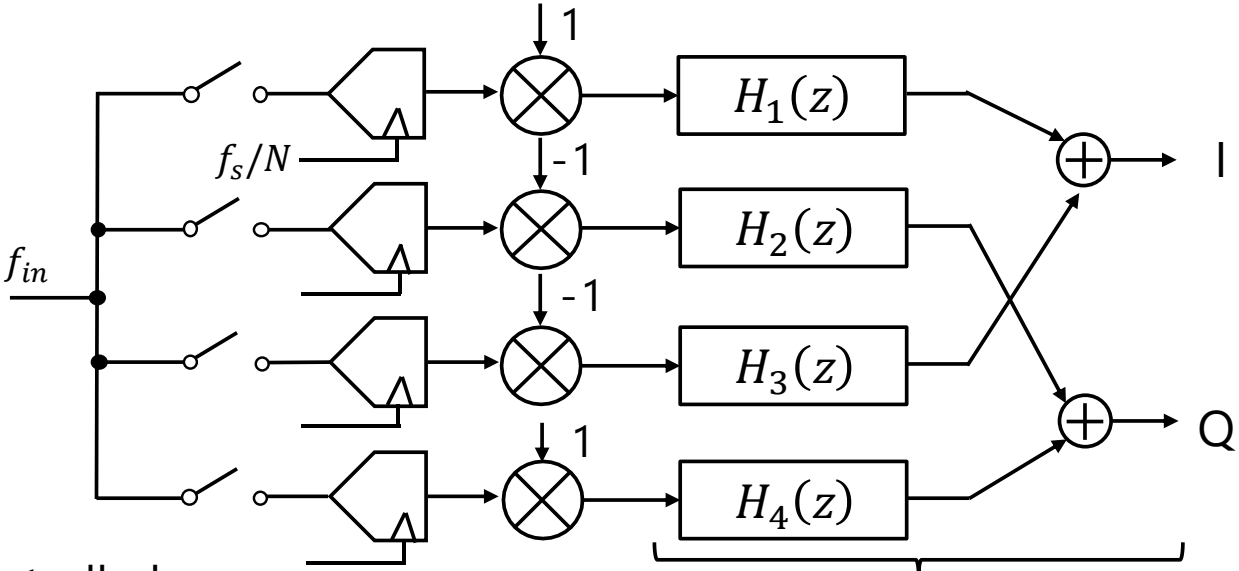


Digital building blocks:

- Operate at gigasamples per second (GS/s) rates
- Consume a large amount of the total power

N: Number of channels, TI: Time-interleaved, ADC: Analog-to-digital converter, CIC: Cascaded integrator-comb, *D*: Decimation factor

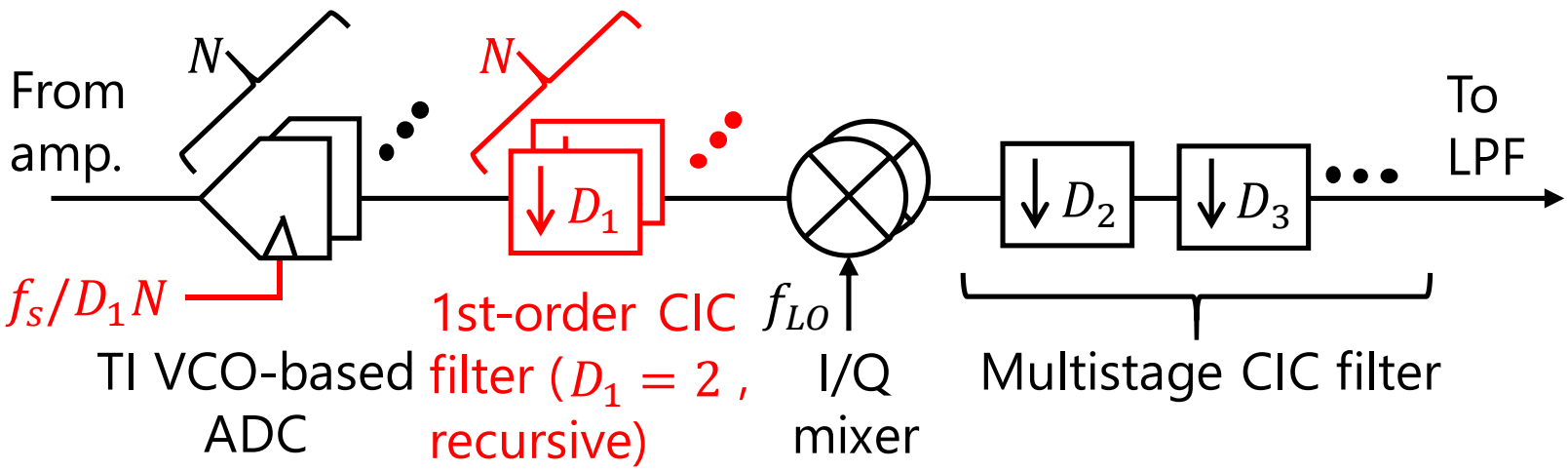
Conventional Methods



- TI VCO-based ADCs achieve high-speed sampling and high resolution with lower power (TCAS-I '08, ISSCC '19)
- $f_s = 4f_{in}$ greatly simplifies I/Q mixers (A-SSCC'11, JSSC '12)
- Polyphase CIC filters relax the speed requirements of the adders (TCAS-II '01, JSSC '12)

Conventional methods have not considered the digital circuits in TI-ADCs and not decreased the power consumption.

Objectives

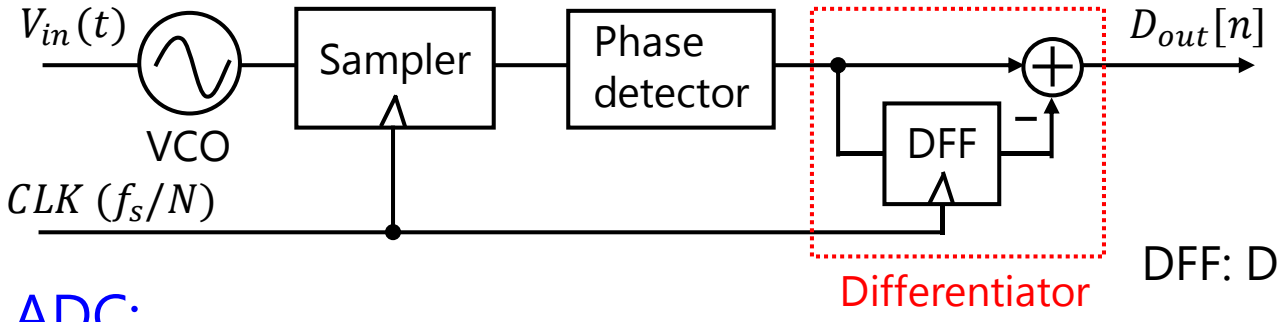


1. Place first-order recursive CIC filters with $D_1 = 2$ after a TI VCO-based ADC:

- Remove the differentiators in the ADC
- Decrease the clock frequencies of the samplers by D_1
- Reduce the total power consumption of the receiver

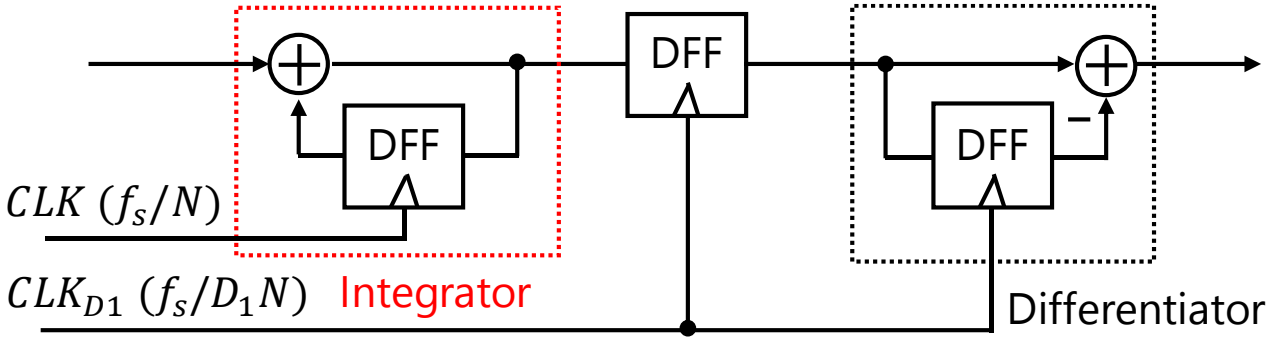
2. Design and simulate a 3.6-GS/s receiver, directly sampling Sub-GHz (900 MHz) signals.

VCO-Based ADC and First-Order Recursive CIC Filter



VCO-based ADC:

- Consists of a sampler, phase detector, and differentiator $(1 - z^{-1})$

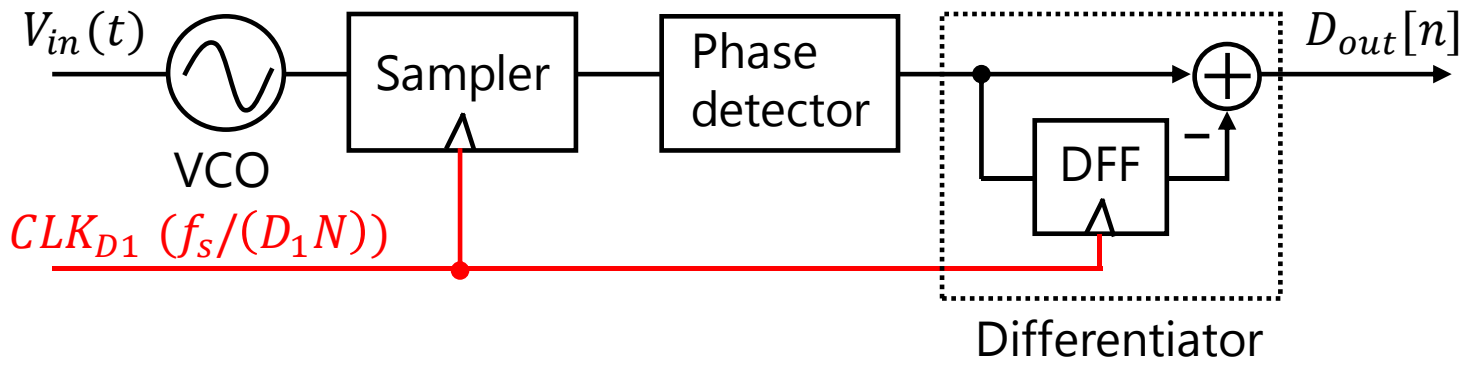


First-order recursive CIC filter ($D_1 = 2$):

- Consists of an integrator $(1/(1 - z^{-1}))$, decimator, and differentiator

1. The differentiator is canceled out by the integrator.
2. The decimator is moved to the sampler.

VCO-Based ADC with First-Order Recursive CIC Filter

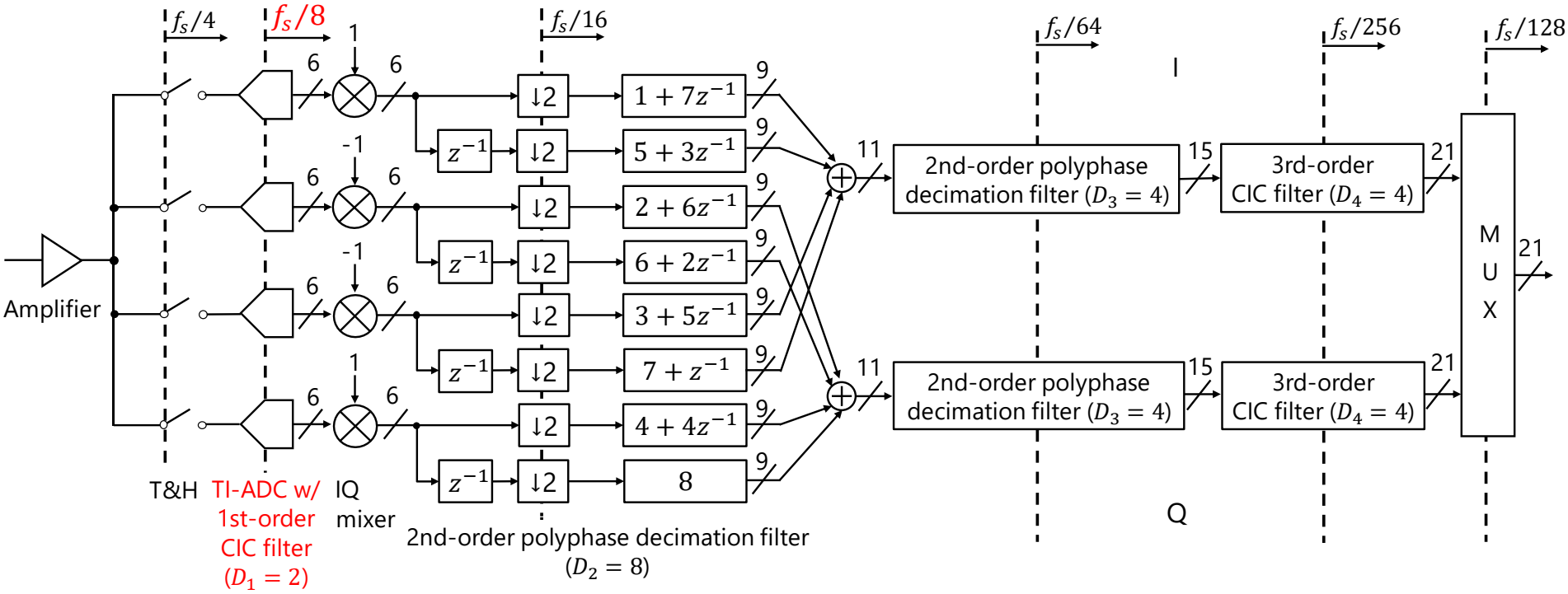


Proposed VCO-based ADC has:

- Sampler and differentiator operating at $f_s/(D_1N)$
- Frequency response of the first-order CIC filter with $D = 2$

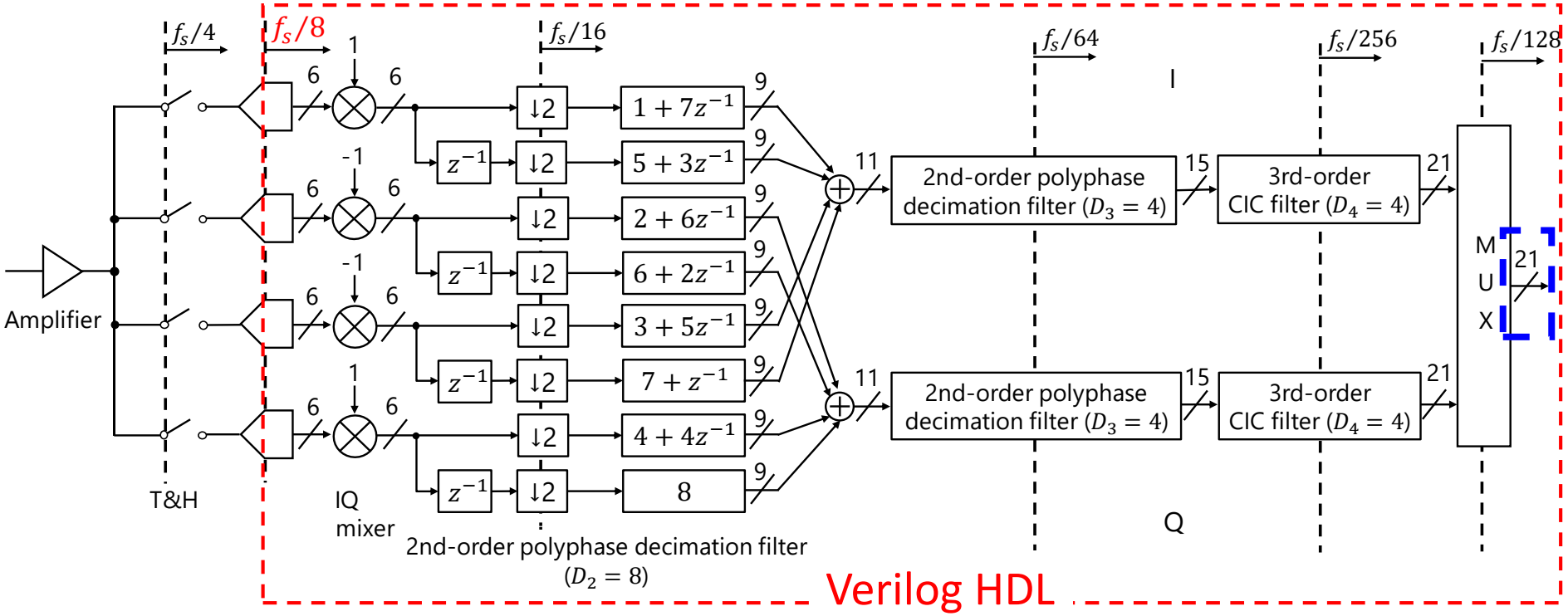
Fewer digital blocks and lower clock frequency reduce the total power consumption of the receiver.

Proposed Direct-RF Sampling Receiver



- Consists of a 4-channel TI VCO-based ADC with 1st-order CIC filters ($D_1 = 2$) and 2nd- and 3rd-order CIC filters
- Decreases the data rate of f_s to $f_s/256$

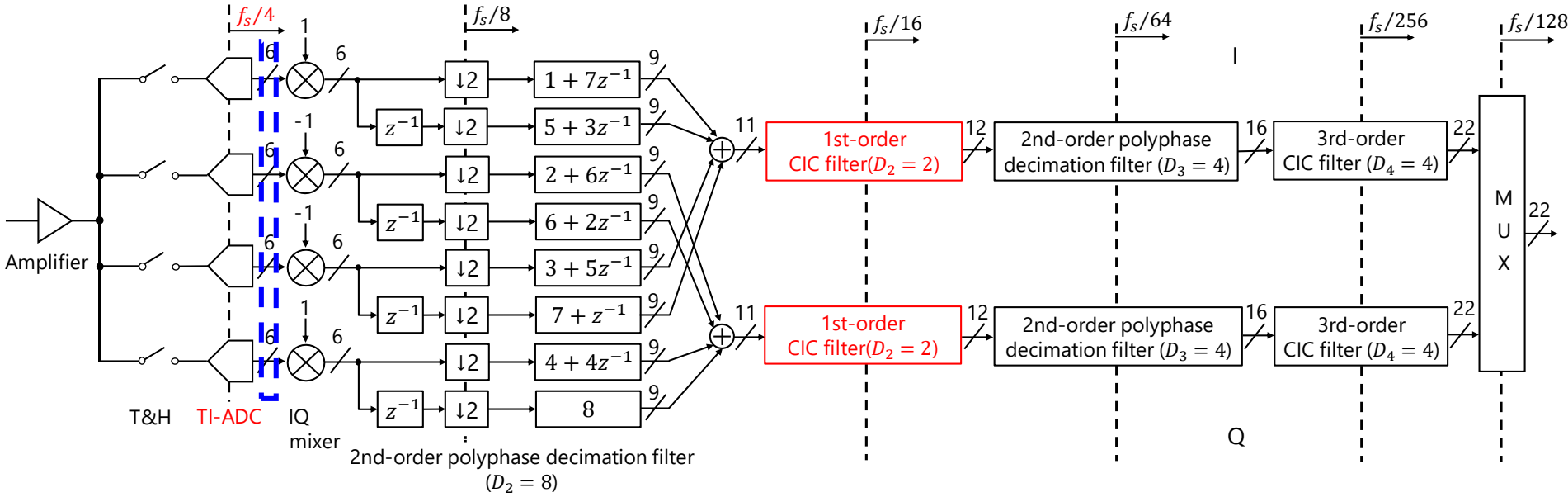
Simulations of Receiver with Proposed Method



- Tools: Mathworks MATLAB/Simulink, Candence NC-Verilog
- Perfomances: SNR, chip area, power consumption

Number of data: N_D	$2^{21}(= 2097{,}152)$
Sampling frequency: f_s	1
Frequency of input signal: $f_{in} = f_s/4 + f_{BB}$	1/4 + 1/8192
Amplitude of input signal: A_{in}	0.20

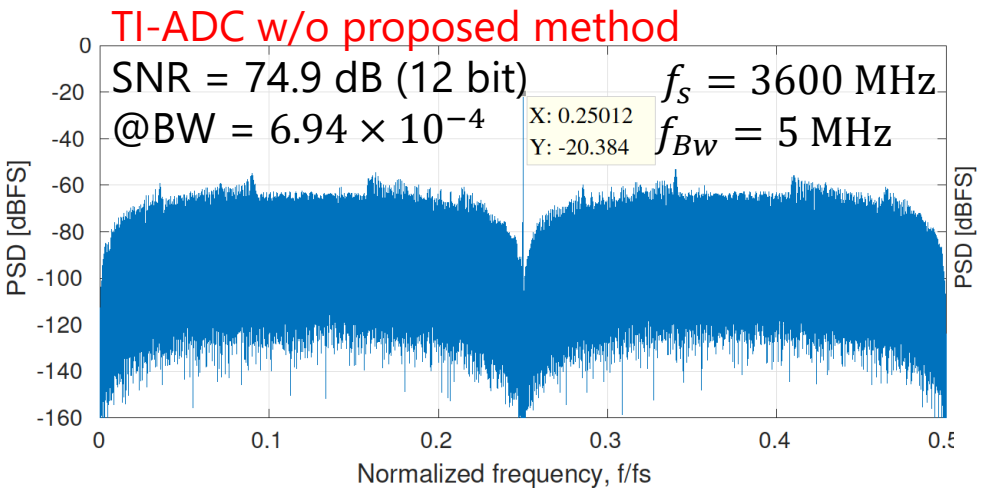
Receiver without Proposed Method (Conv.)

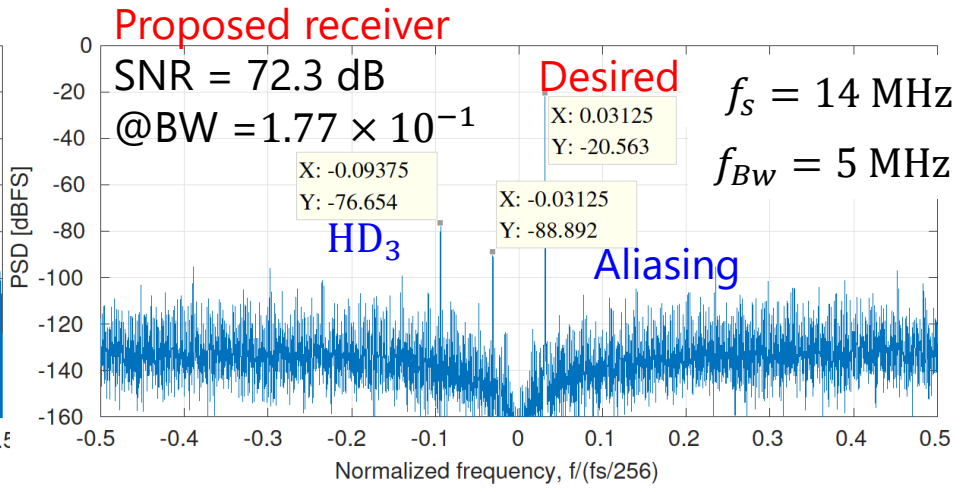


- Sampling rate for one ADC is $f_s/4$.
- First-order recursive CIC filters with D = 2 are placed after a second-order polyphase decimation filter with D = 8.

We compare the perfomances of two receivers with and without the proposed method.

Output FFT Spectrum



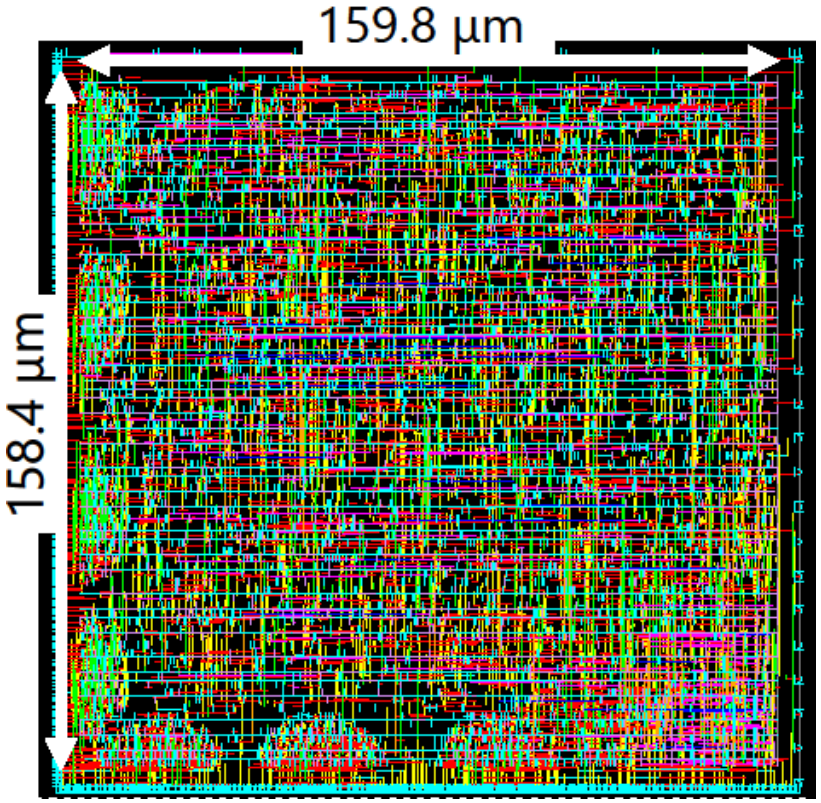


- Desired signal was downconverted to f_{BB}.
- SNR slightly degraded due to the quantization noise folded by decimation in the ADC and CIC filters.
- Aliasing signal (due to mismatch among the ADCs) exsits at $-f_{BB}$
- Third-order harmonic distortion (HD_3) exists at $-3\ f_{BB}$

The proposed receiver operated successfully.

BW: Bandwidth, HD_3: Third-order harmonic distortion

Layout and Chip Area of Digital Blocks



- Process: 65 nm CMOS technology
- Tools: Synopsys Design/IC Compiler
- Condition: (Worst) SS, 0.9-V supply, 125℃,
  (Typ, power consumption only)
  TT, 1.0 V supply, 25℃

Proposed method	Clock rate (Max) [MS/s]	Power consumption [mW]	Chip area [mm^2]
w/	450, 900	3.6, 7.0	0.025
w/o	900	7.2	0.028

The proposed receiver consumes lower power and smaller area.

Performance Comparison of Receivers

	This work	Conv.	E. Martens *et al.*	R. Nanda *et al.*	C. Erdmann *et al.*
Blocks	ADC, Mixer, CIC		Mixer, CIC, HBF	Mixer, CIC, IP, GC, HBF	Mixer, NCO, Decimation, FIFO
CMOS technology [nm]	65		45	65	16 (FinFET)
Sampling rate of TI-ADC [MS/s]	3600,7200	3600	8880	2700	4423
Number of interleaved ADCs	4		6	1	8
Clock rate (Max) [MS/s]	450, 900	900	1480	2700	N/A
Supply voltage [V]	1.0		1.1	1.0	N/A
Power consumption [mW]	3.6, 7.0	7.2	14.3	14	<100
Chip area [mm^2]	0.025	0.028	0.06	0.4	<0.2
Measured	No		Yes	Yes	Yes

- Proposed receiver:
  - Has a half of the clock rate (450 MS/s) and lower power consumption (3.6 mW) compared to the conventional one
  - Operates with the lowest power consumption

HBF: Half band filter, IP: Interpolation, GC: Gain control,
NCO: Numerically controlled oscillator

Summary

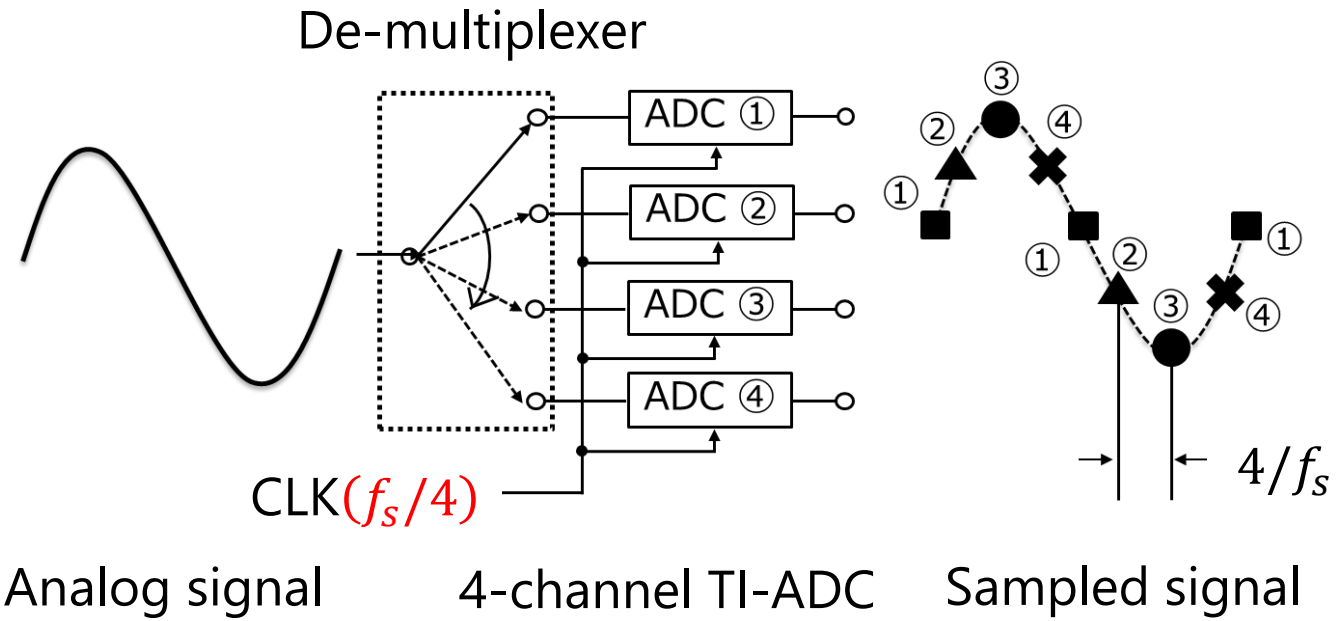
- We place first-order recursive CIC filters with $D = 2$ after TI VCO-Based ADCs in direct-RF sampling receivers.
- The CIC filters remove the differentiators in the VCO-based ADCs and halve the clock frequencies of the samplers.
- We design the digital blocks of a 3.6-GS/s direct-RF sampling receiver in a 65-nm CMOS process.
- Simulations show that the proposed circuit operates at a 450-MS/s rate and consumes 3.6 mW.
- The power consumption is half of the power of the conventional one.

Time-Interleaved ADC (TI-ADC)

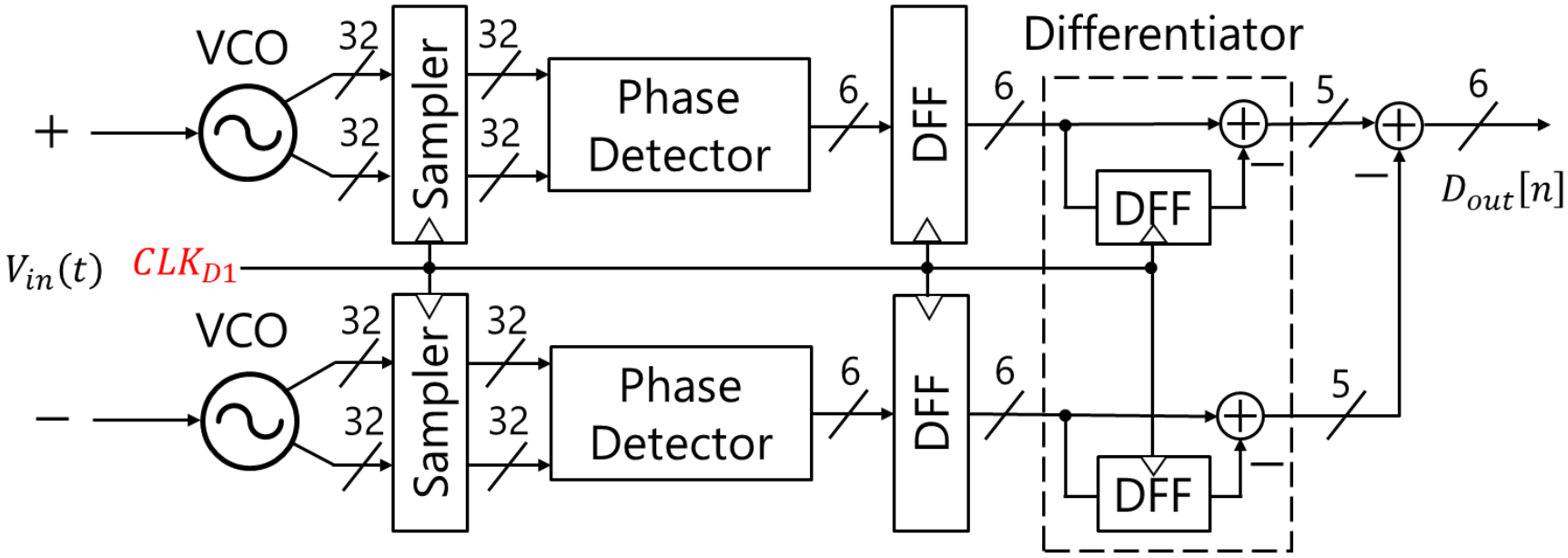
4-channel TI-ADC:

- Converts analog signals to digital ones with four ADCs.
- Decreases the required sampling rate for one ADC to $f_s/4$.

- The sampled signals are multiplexed together to generate a signal sampled at f_s
- This multiplexer can be realized by the addition in the decimation filter



Differential VCO-based ADC

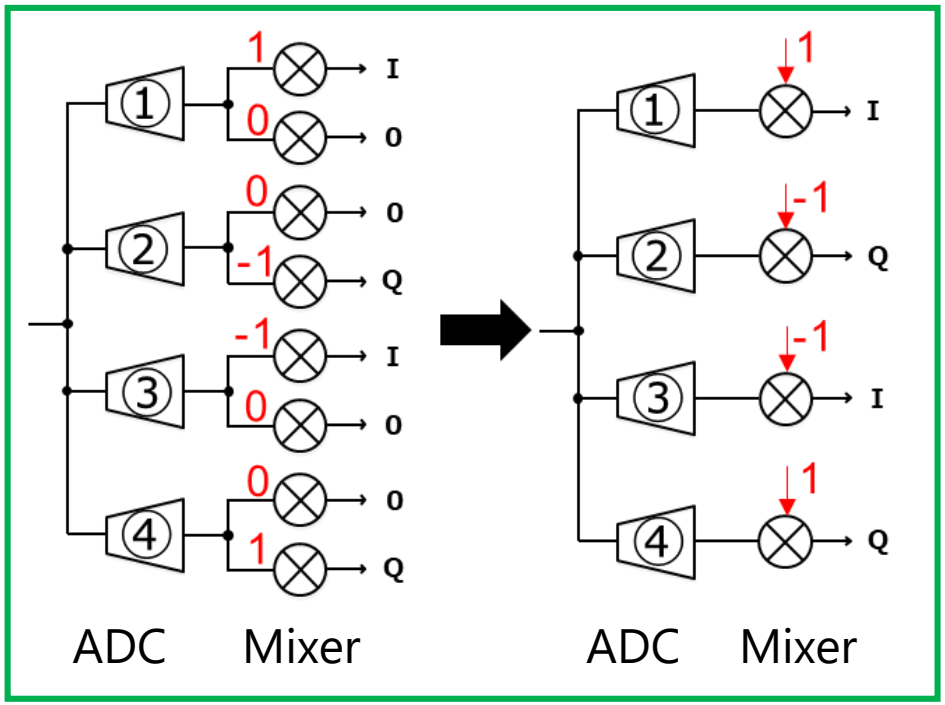


- Adopts a differential topology
- To remove even-order harmonics owing to the nonlinearity of the VCO, consisting of 32 differential delay cells
- The samplers are clocked by a signal with $f_s = 8$ (poposed)
- The phase detector consists of NAND gates and a fat tree encoder.

I/Q Mixer

- Downconverters the digitized signal to baseband with a complex signal, $exp(-j(2\pi f_s/4)t)$

$$e^{-j\left(2\pi\frac{f_s}{4}\right)t}\Big|t = nT_s$$
$$= \underbrace{\cos\left(\frac{\pi}{2}n\right)}_{[1,0,-1,0]} - \underbrace{j\sin\left(\frac{\pi}{2}n\right)}_{[0,-1,0,1]}$$



- Eliminate all mixers using 0 and realize I/Q mixing only with multiplications of 1 and -1

This greatly reduces the hardware cost.