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A Multiband LTE SAW-Less CMOS Transmitter with Source-Follower-Driven Passive Mixers, Envelope-Tracked RF-PGAs, and Marchand Baluns

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SUMMARY We present a multiband LTE SAW-less CMOS transmitter with source-follower-driven passive mixers, envelope-tracked RF-programmable gain amplifiers (RF-PGAs), and Marchand Baluns. A driver stage for passive mixers is realized by a source follower, which enables a quadrature modulator (QMOD) to achieve low noise performance at a 1.2 V supply and contributes to a small-area and low-power transmitter. An envelope-tracking technique is adopted to improve the linearity of RF-PGAs and obtain a better Evolved Universal Terrestrial Radio Access Adjacent Channel Leakage power Ratio (E-UTRA ACLR). The Marchand balun covers more frequency bands than a transformer and is more suitable for multiband operation. The proposed transmitter, which also includes digital-to-analog converters and a phase-locked loop, is implemented in a 65-nm CMOS process. The implemented transmitter achieves E-UTRA ACLR of less than −42 dBc and RX-band noise of less than −158 dBc/Hz in the frequency range of 700 MHz–2.6 GHz. These performances are good enough for multiband LTE and SAW-less operation.

key words: *multiband, LTE, SAW-less, CMOS, transmitter, quadrature modulator, source follower, envelope-tracking, programmable gain amplifier, balun*

1. Introduction

As smart phones become popular, the data traffic increases dramatically. Transceivers which support Long Term Evolution (LTE) systems are in great demand. The LTE system specifies higher peak-to-average power ratio (PAPR) signals and more operating bands than the previous WCDMA/HSPA systems [1]. This requires higher linearity and multiband operations for transmitters. Additionally, the existing demand of SAW-less operation imposes low RX-band noise performance on transmitters. Therefore, LTE transmitters must achieve both high linearity and low noise performance over wideband frequency ranges.

Table 1 shows our objectives of the RX-band noise, linearity, and frequency range. A 3-dB margin is added to a RX-band noise of −155 dBc/Hz calculated in [2] for process, voltage, and temperature variations. To reduce the power consumption of an external power amplifier (PA) and obtain more margins, we tighten the target Evolved Universal Terrestrial Radio Access Adjacent Channel Leakage power Ratio (E-UTRA ACLR) by 2 dB from our previous work [3]. The required frequency ranges are shown in [1].

Table 1 Target performance of multiband LTE SAW-less transmitter.

Performance	RX-band noise	E-UTRA ACLR	Freq.range
Unit	dBc/Hz	dBc	MHz
Value	−158	−42	700~2600

The main challenge for the LTE SAW-less transmitter is to achieve both such a low noise and high linearity with as low power consumption as possible. The 25%-duty-cycle LO (25%LO) passive mixers for a quadrature modulator (QMOD) and passive-RC filters [2], [4]–[6] reduce the noise contributions of RF and base-band blocks, respectively, and enable the transmitter to meet the above noise requirement. However, a driver stage for the passive mixer, which also influences the noise performance, has not been examined.

The PAPR of an LTE signal is about 2.5 dB higher than that of a WCDMA signal. This means that a RF programmable gain amplifier (RF-PGA), which drives a PA, needs higher linearity, i.e., consumes more current (about twice). In addition, a wideband output balun for the RF-PGA is needed for multiband operation. The previous works have not investigated the linearity improvement technique and wideband balun for the RF-PGA.

In this work, we propose a multiband LTE SAW-less CMOS transmitter with source-follower-driven passive mixers, envelope-tracked RF-PGAs, and Marchand baluns [7]. The driver stage for the passive mixer is realized by the source follower. This enables the QMOD to achieve low noise performance and reduces the occupied chip area and power consumption of the transmitter. An envelope-tracking technique is newly adopted to improve the linearity of the previous RF-PGA [3] and obtain a better E-UTRA ACLR without additional power consumption. The Marchand balun is used instead of a transformer for less insertion loss and border 1-dB bandwidth.

This paper is organized as follows. The architecture of the proposed transmitter is shown in Sect. 2. Section 3 describes the QMOD, envelope-tracked RF-PGA, and Marchand balun. Section 4 shows the measurements of the transmitter implemented in a 65-nm CMOS process, and Sect. 5 concludes the paper.

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2. Transmitter Architecture

2.1 Building Blocks of Transmitter

Figure 1 shows a block diagram of the proposed LTE transmitter, based on IQ direct conversion architecture. The transmitter consists of IQ digital-to-analog converters (DACs), active low-pass filters (LPFs), passive-RC filters, a QMOD, a divider, a phase-locked loop (PLL) [8], envelope-tracked RF-PGAs, and Marchand baluns. The QMOD, divider, and PLL operate at 1.2 V supplied by low-dropout (LDO) voltage regulators, while the DACs, active LPFs, and RF-PGAs operate at 2.8 V supplies, because the DACs and active LPFs handle high PAPR LTE signals. For example, if the root mean square (rms) amplitude of the base-band signal, $v_{BB,rms}$, is 0.1 V, the input and output voltage ranges required for the DAC and LPF are calculated as about 1.2 Vpp, where an LTE PAPR and headroom are assumed to be 9.4 dB and 6 dB, respectively.

The DAC with 12 bit resolution and 60∼100-MHz sampling rate converts the digitally modulated signals coming from a digital interface into analog signals. The active LPF has from fifth- to eighth-order Butterworth response to attenuate unwanted alias signals from the DAC. The filter order is adjusted according to the signal bandwidth. The passive-RC filter, whose cut-off frequency is 10 MHz or less (depends on the operating band), reduces the out-of-band noise of the active LPF.

The divider consists of five divide-by-2 dividers and three selectors, and divides the frequency of LO signals coming from the PLL and sends the signals to the QMOD.

The QMOD consists of source followers, passive mixers, and a 25%LO generator. It up-converts IQ base-band signals into RF signals. Two load inductors resonate with the input parasitic capacitances of the RF-PGAs and enable the QMOD to operate in the frequency ranges of 1.4–2.0 GHz and 2.5–2.6 GHz, respectively.

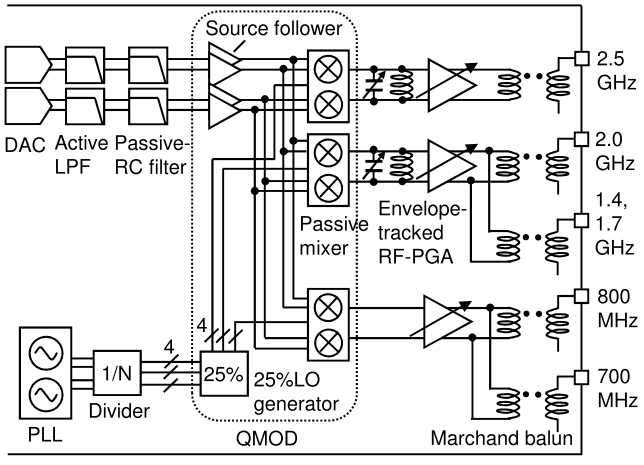

Fig. 1 Block diagram of the proposed LTE transmitter.

The RF-PGA controls the output power with about 78 dB gain range and 0.5 dB gain step. Five baluns provide the differential-to-single-ended conversion for external PAs.

2.2 Noise Consideration

A transmitter with low RX-band noise realizes SAW-less operation. The noise performance is evaluated as CNR:

$$CNR \equiv \frac{P_{out,n}}{P_{out,s}}, \tag{1}$$

where $P_{out,n}$ is the output noise power in the RX band and $P_{out,s}$ the output signal power. We use the following four approaches to achieve such a low CNR:

1. Large amplitude base-band signal,
2. Passive-RC filter,
3. Passive mixer,
4. Single-stage RF-PGA.

First, a large amplitude base-band signal leads to a low CNR. The CNR of a MOSFET is expressed as

$$CNR_{Tr} = \frac{4k_BT\gamma g_m}{g_m^2 v_{BB,rms}^2} = \frac{4k_BT\gamma}{g_m v_{BB,rms}^2}, \tag{2}$$

where k_B is Boltzmann's constant, T the absolute temperature, γ noise parameter (2/3 for long-channel MOSFETs), g_m the transconductance of the common-source transistor. Equation (2) shows that a larger $v_{BB,rms}$ results in a lower CNR. Therefore, a large amplitude base-band signal reduces the noise contributions of the circuit blocks and improves the noise performance of the transmitter. The upper limit of $v_{BB,rms}$ is determined by the linearity of the circuit and the PAPR of the signal.

Second, the passive-RC filter decreases the out-of-band noise from the active LPF. The CNR of the active LPF, based on common-source amplifiers, is also expressed as Eq. (2), which means that a lower CNR requires a larger g_m, i.e., more current consumption. By employing the passive-RC filter with a cutoff frequency of a signal bandwidth, we can reduce the out-of-band noise of the active LPF without additional current consumption.

Third, the passive mixer has better noise performance than an active mixer. The transistor of the passive mixer operates in the deep triode region, i.e., operates as a switch, whereas that of the active mixer in the saturation region. By using a 65-nm or less CMOS process, we can easily achieve a switch transistor with a small on-resistance ($< 10\,\Omega$). This allows the passive mixer with lower noise than the active mixer.

Finally, the single-stage RF-PGA achieves less noise, compared to a multi-stage RF-PGA. For example, in the case of a two-stage PGA, the output noise of the first stage is amplified by the second stage, and then it is added to the output noise of the second one. When the CNR of the first stage is equal to that of the second one, the total CNR of the two-stage PGA degrades by 3 dB. To reduce the noise contribution from the second stage, we need much current for

the stage.

3. Circuit Design

In this section, we show the building blocks of the transmitter: QMOD, enveloped-tracked RF-PGA, and Marchand balun.

3.1 QMOD with Source-Follower-Driven Passive Mixer

The proposed QMOD consists of source followers, passive mixers, and a 25%LO generator, as shown in Fig. 1. Figure 2 shows the detailed schematics of the QMOD and the waveform of 25%LO signals. The 25%LO passive mixer can achieve both high linearity and low noise performance at a low supply. The 25%LO generator is composed of four AND gates [9] and generates the 25%LO signals by using quadrature LO signals provided by a divider.

A key building block in the QMOD is a driver stage for the passive mixer. The input impedance of the passive mixer is relatively low due to the input capacitance of the RF-PGA. The previously reported configuration [2], [6], in which the active LPF with the passive-RC filter drives the passive mixer, consumes large chip area and high power consumption to drive such a low impedance; A small resistor is required for the passive-RC filter to prevent the signal reduction at the input of the passive mixer, which results in a large capacitor (large area) for the RC filter; The active LPF requires a high supply voltage for LTE operation as shown in the previous section and its output buffer consumes large current.

In this work, the source follower is used as the driver stage for the passive mixer, as shown in Fig. 3. The advantages of the source follower are shown in Table 2.

First, the power consumption to drive the passive mixers decreases. The source follower can drive a low impedance and deal with high-PAPR LTE signals at a low supply voltage (1.2 V). The LTE signal imposes a wide input voltage range on the drive stage. Although the source follower has both large current gain and low output impedance, its input voltage range is narrow if its input is biased by $V_{DD}/2$, where V_{DD} is the supply voltage. Biased by a higher voltage, the source follower has wider input voltage range. The allowable maximum and minimum input voltages of the source follower are given by

$$V_{in,SF,max} = V_{DD} + V_{th1}, \tag{3}$$

$$V_{in,SF,min} = V_{gs1} + V_{ds2,sat}, \tag{4}$$

respectively, where V_{th1} is the threshold voltage of the input transistor, M_1, V_{gs1} the gate-source voltage of M_1, and $V_{ds2,sat}$ the saturated drain-source voltage of the current source transistor, M_2. Equations (3) and (4) mean that the input voltage range can be maximized by biasing the input of the source follower by $(V_{in,SF,max} + V_{in,SF,min})/2$. Considering the bias conditions for M_1 and M_2, we bias the input by 0.9 V in this design. This enables the source follower to drive the passive mixer for LTE operation even at a 1.2 V supply. In this way, the driver stage for the passive mixer consumes current (~ 3 mA) from a 1.2 V supply instead of a 2.8 V one, and then the power consumption of the transmitter decreases.

Second, the chip area of the passive-RC filter decreases. The source follower provides a high load impedance for the passive-RC filter. The input impedance of the source follower is very high. This allows the design of a passive-RC filter with a large resistor (R) and small capacitor (C), because no signal reduction occurs at the input of the source follower. For example, in the case of a passive-RC filter with a cut-off frequency of 10 MHz, $R = 100\,\Omega$ and $C = 150$ pF are used for the filter without the source follower, while $R = 3\,\mathrm{k}\Omega$ and $C = 5$ pF used for the filter with the source follower. Thus, the source follower separates the passive-RC filter from the passive mixer and contributes to a small-area transmitter.

Simulations show that the proposed QMOD achieves a

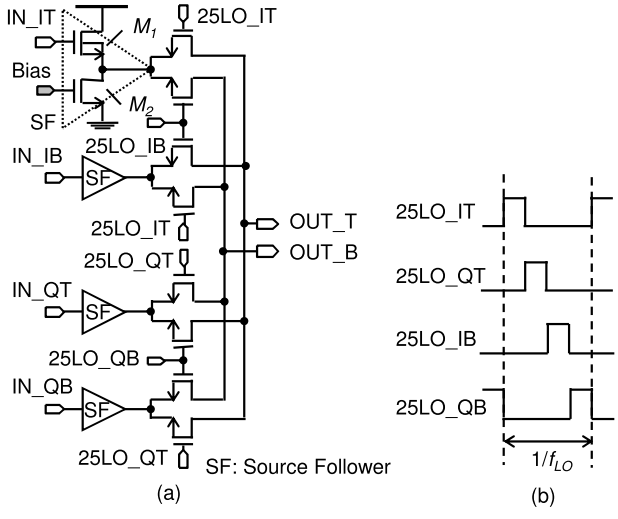

Fig. 2 (a) Schematic of the proposed QMOD and (b) the waveform of 25%LO signals.

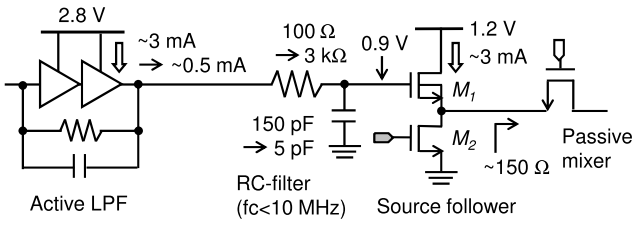

Fig. 3 Proposed driver stage for the passive mixer.

Table 2 Reduction of power consumption and area by source follower (SF).

Item	Without SF	With SF	Reduction of power/area
Power consumption to drive passive mixer	4×3 mA from 2.8 V	4×3 mA from 1.2 V	19.2 mW
Capacitance for passive-RC filter	4×150 pF	4×5 pF	0.2 mm^2

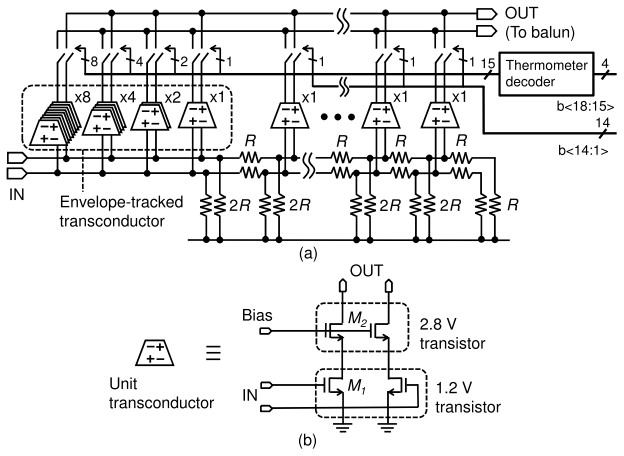

Fig. 4 (a) Block diagram of the RF-PGA and (b) schematic of the transconductor.

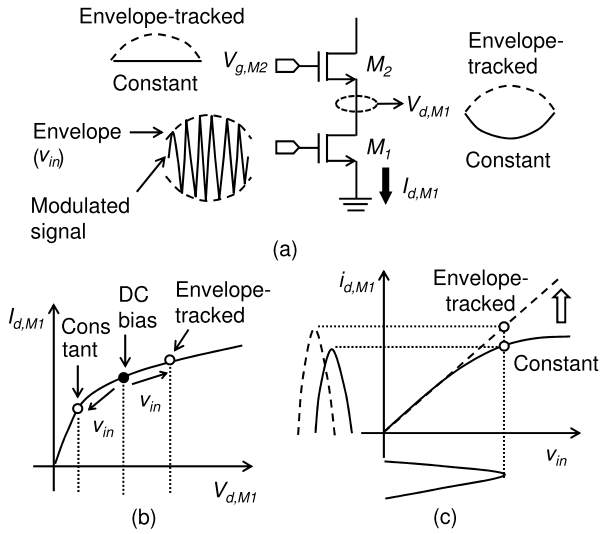

Fig. 5 Concept of envelope-tracked biasing: (a) Transconductor with envelope-tracked or constant biasing, (b) $I_{d,M1}$ versus $V_{d,M1}$, and (c) $i_{d,M1}$ versus v_{in}.

CNR of −163 dBc/Hz and an E-UTRA ACLR of −48 dBc with a current consumption of 17.5 mA including the 25%LO generator for Band 1.

3.2 Envelope-Tracked RF-PGA

The RF-PGA consists of fifteen thermometer-weighted transconductors and fourteen binary-weighted transconductors with R-2R ladders, as shown in Fig. 4(a). The gain control scheme is described in detail in [3]. The transconductor is composed of two common-source and cascode transistors, as shown in Fig. 4(b). The cascode transistor, M_2, improves the isolation between the input and output terminals, while causing the linearity degradation. When a high-PAPR LTE signal enters the common-source transistor, M_1, the drain voltage of M_1 decreases and then the drain current of M_1 decreases. A higher gate bias voltage for M_2 prevents the degradation, but leads to more current consumption.

In this work, we employ an envelope-tracking technique, i.e., "envelope-tracked biasing", on the thermometer-weighted transconductors to improve the linearity. Envelope-tracking techniques have been mainly applied to PAs [10], [11]; The supply voltage which tracks the envelope of a modulated signal improves the linearity of the amplifier. In this design, the envelope-tracking technique is used to bias the cascode transistor in the thermometer-weighted transconductor, which deals with large input voltage swings. This improves the linearity of the transconductor with no additional power consumption.

Figure 5 illustrates the concept of the envelope-tracked biasing. This biasing makes the gate voltage of M_2, $V_{g,M2}$, track to the envelope of an input modulated signal, v_{in}, as shown in Fig. 5(a). Accordingly, the drain voltage of M_1, $V_{d,M1}$, also tracks to the envelope. In the case of the constant biasing for M_2 (without the envelope-tracked biasing), $V_{d,M1}$ decreases as v_{in} increases.

The v_{in} dependence of $V_{d,M1}$ affects the linearity of M_1. Figure 5 (b) shows the drain current of M_1, $I_{d,M1}$, versus $V_{d,M1}$. As $V_{d,M1}$ increases, $I_{d,M1}$ gradually increases due to the channel-length modulation of M_1. For the constant biasing, $V_{d,M1}$ decreases according to v_{in} and then $I_{d,M1}$ decreases from a DC bias current, shown as a dot in Fig. 5(b). In contrast to this, for the envelope-tracked biasing, $I_{d,M1}$ increases from the DC bias current. Figure 5 (c) shows the small-signal characteristic of $I_{d,M1}$, $i_{d,M1}$, versus v_{in}. The constant biasing causes the reduction of $I_{d,M1}$ for the peak of v_{in}, resulting in a nonlinear characteristic of $i_{d,M1}$. Meanwhile, the envelope-tracked biasing prevents the current reduction and then provides better linearity.

To express the linearity improvement analytically, we define $I_{d,M1}$ as

$$I_{d,M1} = \frac{\beta_{M1}}{2}\left(v_{in} + V_{od,M1}\right)^2\left(1 + \lambda V_{d,M1}\right), \tag{5}$$

where β_{M1} is the transconductance parameter of M_1, $V_{od,M1}$ the overdrive voltage of M_1, and λ the channel-length modulation coefficient of M_1. The drain voltage of M_1, $V_{d,M1}$, can be expressed as

$$V_{d,M1} = \alpha v_{in} + \beta, \tag{6}$$

where α and β are coefficients which depend on the bias condition for M_2. For the envelope-tracked biasing, α is positive (> 0), while α equals -1 for the constant biasing, as illustrated in Fig. 5(a). From Eqs. (5) and (6), $i_{d,M1}$ can be derived as

$$i_{d,M1} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3, \tag{7}$$

where a_1, a_2, and a_3 represent the linear, second-order, and third-order coefficients of $i_{d,M1}$, respectively. Table 3 shows the comparison of a_1, a_3, and a_1/a_3 for the envelope-tracked and constant biasing. The linearity of an amplifier such as 1-dB compression point (CP1 dB) and third intercept point are proportional to squared a_1/a_3 [12]. The envelope-tracked biasing generates $\alpha > 0$ and prevents gain (a_1) reduction due

Table 3 Comparison of coefficients for envelope-tracked and constant biasing.

	Envelope-tracked biasing	Constant biasing
a_1	$\alpha\lambda V_{od,M1}^2$ $+2(\beta\lambda+1)V_{od,M1}$	$-\lambda V_{od,M1}^2$ $+2(\beta\lambda+1)V_{od,M1}$
a_3	$\alpha\lambda$	$-\lambda$
a_1/a_3	$V_{od,M1}^2 + \frac{2}{\alpha}\left(\beta+\frac{1}{\lambda}\right)V_{od,M1}$	$V_{od,M1}^2 - 2\left(\beta+\frac{1}{\lambda}\right)V_{od,M1}$

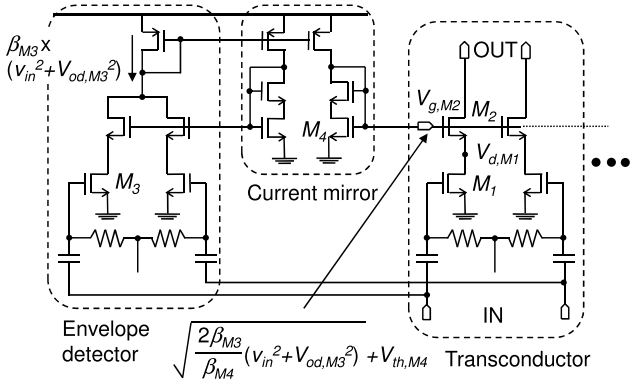

Fig. 6 Schematic of the envelope-tracked biasing circuit applied to the transconductors.

to nonlinearity, resulting in larger a_1/a_3 (higher linearity) than the constant biasing.

Figure 6 shows the schematic of the envelope-tracked biasing circuit, which consists of the envelope detector and current mirror circuit. The detector, which is a kind of a squaring circuit, generates current according to the envelope of the input modulated signal:

$$I_{env,det} = \beta_{M3}\left(v_{in}^2 + V_{od,M3}^2\right), \tag{8}$$

where $V_{od,M3}$ is the overdrive voltage of M_3. By utilizing the current, the current mirror makes $V_{g,M2}$ track to the envelope:

$$\begin{aligned} V_{g,M2} &= \sqrt{\frac{2\beta_{M3}}{\beta_{M4}}\left(v_{in}^2 + V_{od,M3}^2\right)} + V_{th,M4} \\ &= \sqrt{\frac{2\beta_{M3}}{\beta_{M4}}}v_{in}\left(1 + \frac{V_{od,M3}^2}{2v_{in}^2} + \cdots\right) + V_{th,M4} \\ &\approx \sqrt{\frac{2\beta_{M3}}{\beta_{M4}}}v_{in} + V_{th,M4} \propto v_{in}, \end{aligned} \tag{9}$$

where β_{M4} is the transconductance parameter of M_4, $V_{th,M4}$ the threshold voltage of M_4, and the approximation is valid when $V_{od,M3}$ is smaller than v_{in}. This condition is satisfied, because the gate of M_3 is biased at a low voltage to ensure that the envelope detector provides a squaring function. In this way, the envelope-tracked biasing circuit generates $V_{g,M2}$ proportional to the envelope.

The effect of the envelope-tracked biasing can be maximized by minimizing α, because the third-order nonlinearity, a_3, is proportional to α as shown in Table 3. This means

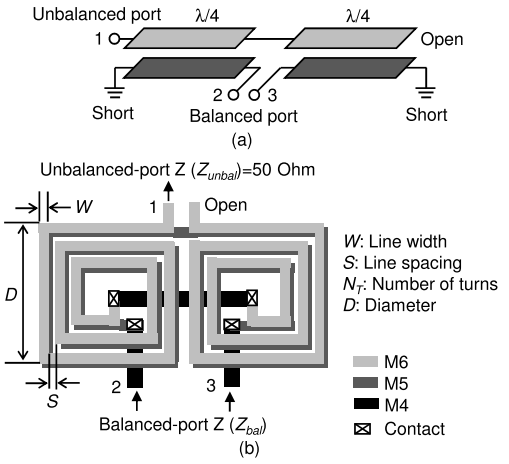

Fig. 7 (a) Marchand balun with $\lambda/4$ coupled lines and (b) top view of a stacked Marchand balun.

that designing the biasing circuit to suppress the fluctuation of $V_{d,M1}$ ($= \alpha v_{in} + \beta$) leads to higher linearity. From Eq. (9), we can achieve the maximum effect by decreasing β_{M3} and increasing β_{M4}.

Simulations show that the RF-PGA with the envelope-tracked biasing obtains an output CP1 dB (OCP1 dB) of +14.8 dBm for an output power of +3.4 dBm. This OCP1 dB is 5.7 dB higher than that of the RF-PGA with the constant biasing. The current consumption of the envelope-tracked RF-PGA is about 32 mA for an output power of +3 dBm for Band 1.

3.3 Marchand Balun

The Marchand balun with $\lambda/4$ coupled lines, shown in Fig. 7, is adopted for differential-to-single-end conversion of the RF-PGA. A spiral configuration increases the mutual inductance and capacitance between the transmission lines, and then the Marchand balun with spiral lines achieves much smaller area than one with straight lines [13], [14]. In this paper, the two spiral lines with balanced and unbalanced ports are completely stacked as show in Fig. 7(b) to further increase the mutual capacitance and reduce the chip area. An M6 layer is used for the upper winding, an M5 layer for the lower one, and M4 layers for the connection between left and right slides and the inputs of the balanced ports.

The Marchand balun has less insertion loss ($-|S_{12}|$) and broader 1-dB bandwidth than a 1:1 transformer. Generally, the insertion loss of the balun or transformer is determined by the coupling factor k and the quality factor Q of the line (spiral inductor). To reduce the insertion loss of the transformer, we need to increase k as much as possible (i.e., the minimum loss is achieved for $k = 1$) [15]. On the other hand, in the case of the Marchand balun, there is the optimum k for the insertion loss. This value, which changes with the Q of the line, is calculated as $1/\sqrt{3}$ (≈ 0.57) for the lossless line [14], [16]. This means that a Marchand balun with a reasonable k ($0.6 \sim 0.8$) can achieve less insertion

Table 4 Performance comparison of a 2.0-GHz Marchand balun and 1:1 transformer.

Performance	Marchand	Transformer
Chip area [um^2]	$\sim 140 \times 300$	$\sim 130 \times 280$
Balance-port impedance (Z_{bal})	~ 280 (depends on k)	~ 70 ($N_T \times k \times Z_{unbal}$)
Reflection ($\lvert S_{11} \rvert$) [dB]	-14	-7
Insertion loss ($-\lvert S_{12} \rvert$) [dB]	~ 2	~ 3 ($\propto k$)
1-dB bandwidth [MHz]	~ 500	~ 350
Gain imbalance [dB]	~ 1	~ 0.1
Phase imbalance [deg.]	± 5	± 10
CMRR [dB]	< -20	< -20

Z_{unbal}: Unbalanced-port impedance, N_T: Number of turns

loss than the transformer.

Table 4 shows the performance comparison of a 2.0-GHz Marchand balun and 1:1 transformer with the same configuration as Fig. 7(b). A 2.5-D electromagnetic simulator (Agilent Momentum) is used for the simulation. We determine the design parameters of the baluns (line width, line spacing, and number of turns) to have a small area, considering the insertion loss and self-resonance frequency. Simulations show that the Marchand balun achieves less insertion loss and broader 1-dB bandwidth than the transformer with a comparable area. The disadvantage of the Marchand balun is a high balanced-port impedance ($Z_{bal} > 200\,\Omega$). This leads to a large voltage swing at the output of the RF-PGA and causes the linearity degradation. This is not a problem because the RF-PGA operates at a 2.8 V supply and has enough voltage headroom. Additionally, the envelope-tracked biasing, described in Sect. 3.2, improves the linearity of the RF-PGA.

4. Experimental Results

The complete transmitter was implemented in a 65-nm CMOS process with a thick metal layer and metal-insulator-metal (MIM) capacitors. A microphotograph of the fabricated transmitter is shown in Fig. 8. The chip area was 4.5 mm^2. The chip was mounted to a ball grid array (BGA) package. All measurements were obtained by using the internal PLL.

4.1 ACLR and EVM

Figure 9 shows the measured E-UTRA ACLR for an LTE modulated (16 QAM) signal with a bandwidth (BW) of 20 MHz and 100 resource blocks (RBs) in Band 1. The transmitter obtained an E-UTRA ACLR of -42 dBc with an output power of +2.1 dBm. The envelope-tracked biasing (represented by "Envelope ON" in Fig. 9) improved the ACLR by about 3 dB compared to that without the biasing ("Envelope OFF" in Fig. 9).

Figure 10 shows the measured error vector magnitude (EVM) for the same LTE signal and output power as Fig. 9. The average EVM was 2.8% for envelope ON or OFF. The envelope-tracked biasing does not degrade the EVM performance of the transmitter.

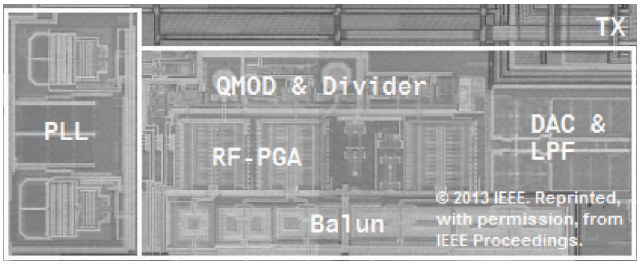

Fig. 8 Microphotograph of the fabricated transmitter.

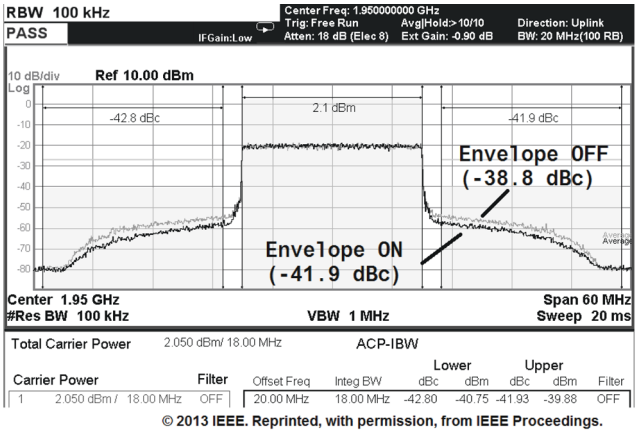

Fig. 9 Measured E-UTRA ACLR for an LTE signal with 20 MHz BW and 100 RBs in Band 1.

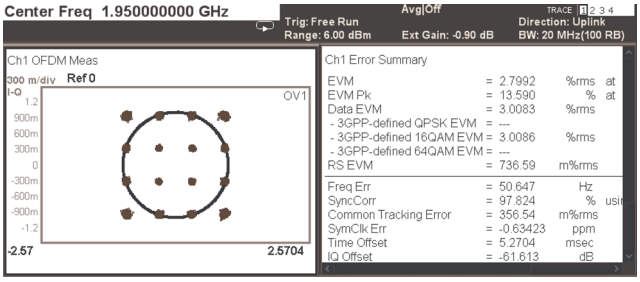

Fig. 10 Measured EVM for an LTE signal with 20 MHz BW and 100 RBs in Band 1.

Figure 11 shows the summary of the measured E-UTRA ACLR and EVM for output powers of +2 dBm in various frequency bands. LTE signals with BW of 5 MHz and 20 MHz were used for the frequency ranges of 700 MHz–1.4 GHz and 1.7 GHz–2.6 GHz, respectively. The transmitter achieved E-UTRA ACLR of less than -42 dBc and EVM of less than 3% in the frequency range of 700 MHz–2.6 GHz. The required E-UTRA ACLR (-42 dBc shown in Sect. 1) and 3GPP EVM specification ($< 12.5\%$ [17]) are satisfied.

4.2 RX-Band Noise

The CNR of the transmitter was measured in the frequency range of 700 MHz–2.6 GHz and shown in Fig. 12. The best noise performance, a CNR of -161 dBc/Hz, was achieved

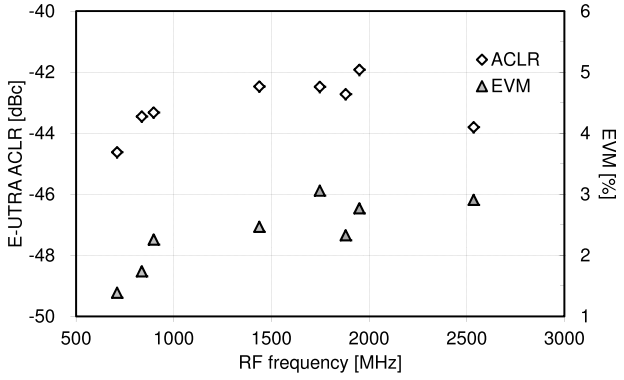

Fig. 11 Measured ACLR and EVM in various frequency bands.

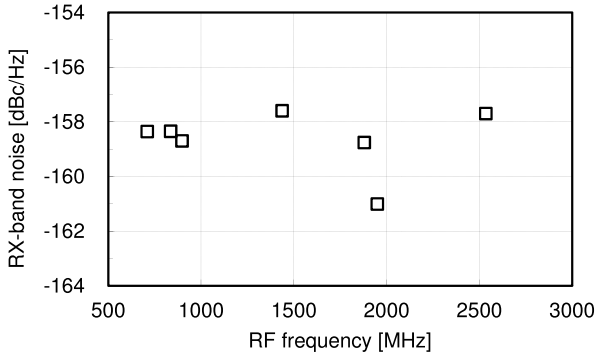

Fig. 12 Measured RX-band noise in various frequency bands.

for Band 1 (1950 MHz), because the duplex frequency is the highest (190 MHz offset). For the other bands, the measured CNR was about −158 dBc/Hz. These performances are enough for SAW-less operation.

4.3 Third Counter-Intermodulation (C-IM3)

For LTE systems, the third counter-intermodulation (C-IM3) products of transmitters generate various unwanted spurs and should be as small as possible [18]. The C-IM3 is the spur at $f_{LO} - 3f_{BB}$, where f_{LO} and f_{BB} are LO and base-band frequencies, respectively, It is mainly caused by the intermodulation of the wanted signal ($f_{LO} + f_{BB}$) and the third-order harmonics (HD3, $3f_{LO} - f_{BB}$) of the QMOD. In this design, the HD3 of the QMOD is reduced to less than −20 dBc by using the load inductor and variable capacitor as shown in Fig. 1.

Figure 13 shows the measured C-IM3 for an LTE signal with BW of 20 MHz and 1 RB in Band 1. The measured C-IM3 was −54 dBc.

4.4 Comparison

Table 5 shows the performance comparison with the previously reported LTE SAW-less transmitters [6], [18] for Band 1. Reference [6] does not have DACs and a PLL, and Ref. [18] does not include a PLL. They degrade the CNR by 1 or 2 dB, which depends on the PLL design and TX-RX offset frequency. Although the proposed transmitter includes the DACs and PLL, it achieves the comparable RX-band noise and best E-UTRA ACLR for Band 1.

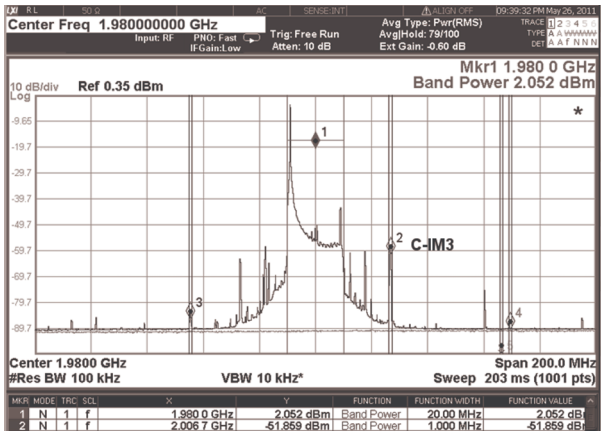

Fig. 13 Measured C-IM3 for an LTE signal with 20 MHz BW and 1 RB in Band 1.

Table 5 Performance comparison of LTE transmitters for Band 1.

	This work	IMEC [6]*	Fujitsu [18]†
Technology	65 nm CMOS	40 nm CMOS	90 nm CMOS
Output power [dBm]	2.1	2.1	4.0
E-UTRA ACLR [dBc]	−42	−39	−40
EVM [%]	2.8	2.5	1.0
RX-band noise [dBc/Hz]	−161	−160	−162
C-IM3 [dBc]	−54	N/A	−62
Current from 1.2 V/2.8 V, 1.1 V/2.5 V in [6], 1.55 V/2.7 V in [18] [mA]	27/44†	25/40	38/52
Chip area [mm^2]	4.5	0.98	5.0

* Without DACs and PLL, †Without PLL

5. Conclusion

We have demonstrated a multiband SAW-less CMOS transmitter for LTE systems. A source follower, which drives 25%LO passive mixers, reduces the chip area and current consumption of passive-RC and active filters, respectively, contributing to a small-area and low power transmitter. An envelope-tracked biasing employed in RF-PGAs improves the linearity, decreasing the E-UTRA ACLR of the transmitter by about 3 dB. A stacked Marchand balun provides less insertion loss and broader 1-dB bandwidth than a transformer, and is more suitable for wideband and multiband operations. The proposed transmitter implemented in a 65-nm CMOS process achieves E-UTRA ACLR of less than −42 dBc and RX-band noise of less than −158 dBc/Hz in the frequency band of 700 MHz–2.6 GHz. These performances are good enough for multiband LTE and SAW-less operation.

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References

[1] A. Pärssinen, "Multimode-multiband transceivers for next generation of wireless communications," Proc. IEEE European Solid-State Circuits Conf., pp.25–36, Helsinki, Finland, Sept. 2011.

[2] M. Ingels, V. Giannini, J. Borremans, G. Mandal, B. Debaillie, P.V. Wesemael, T. Sano, T. Yamamoto, D. Hauspie, J.V. Driessche, and J. Craninckx, "A 5 mm^2 40 nm LP CMOS transceiver for a software-defined radio platform," IEEE J. Solid-State Circuits, vol.45, no.12, pp.2794–2806, Dec. 2010.

[3] M. Mizokami, Y. Furuta, T. Maruyama, and H. Sato, "A 78 dB dynamic range, 0.27 dB accuracy, single-stage RF-PGA using thermometer-weighted and binary-weighted transconductors for SAW-less WCDMA/LTE transmitters," Symp. VLSI Circuits Dig. Tech. Papers, pp.131–132, Honolulu, HI, June 2010.

[4] X. He and J. van Sinderen, "A low-power, low-EVM, SAW-less WCDMA transmitter using direct quadrature voltage modulation," IEEE J. Solid-State Circuits, vol.44, no.12, pp.3448–3458, Dec. 2009.

[5] K. Hausmann, J. Ganger, M. Kirschenmann, G.B. Norris, W. Shepherd, V. Bhan, and D.B. Schwartz, "A SAW-less CMOS TX for EGPRS and WCDMA," IEEE Radio Frequency Integrated Circuits Symp. Dig. Papers, pp.25–28, Anaheim, CA, May 2010.

[6] V. Giannini, M. Ingels, T. Sano, B. Debaillie, J. Borremans, and J. Craninckx, "A multiband LTE SAW-less modulator with −160 dBc/Hz RX-band noise in 40 nm LP CMOS," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp.374–375, San Francisco, CA, Feb. 2011.

[7] T. Kihara, T. Sano, M. Mizokami, Y. Furuta, T. Nakamura, M. Hokazono, T. Maruyama, K. Toyota, K. Maeda, Y. Akamine, T. Yamawaki, T. Heima, K. Hori, and H. Sato, "A multiband LTE SAW-less CMOS transmitter with source-follower-drived passive mixers, envelope-tracked RF-PGAs, and Marchand baluns," IEEE Radio Frequency Integrated Circuits Symp. Dig. Papers, pp.399–402, Montreal, QB, June 2012.

[8] K. Ueda, T. Uozumi, R. Endo, T. Nakamura, T. Heima, and H. Sato, "A digital PLL with two-step closed-locking for multi-mode/multi-band SAW-less. transmitter," Proc. IEEE Custom Integrated Circuits Conf., San Francisco, CA, M-18, Sept. 2012.

[9] D. Kaczman, M. Shah, M. Alam, M. Rachedine, D. Cashen, L. Han, and A. Raghavan, "A single-chip 10-band WCDMA/HSDPA 4-band GSM/EDGE SAW-less CMOS receiver with DigRF 3G interface and +90 dBm IIP2," IEEE J. Solid-State Circuits, vol.44, no.3, pp.718–739, March 2009.

[10] G. Hanington, P.F. Chen, P.M. Asbeck, and L.E. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications," IEEE Trans. Microw. Theory Tech., vol.47, no.8, pp.1471–1476, Aug. 1999.

[11] F. Wang, A.H. Yang, D.F. Kimball, L.E. Larson, and P.M. Asbeck, "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," IEEE Trans. Microw. Theory Tech., vol.53, no.4, pp.1244–1255, April 2005.

[12] B. Razavi, RF Microelectronics, 2nd ed., Prentice Hall PTR, Upper Saddle River, NJ, 2011.

[13] Y.J. Yoon, Y. Lu, R.C. Frye, M.Y. Lau, P.R. Smith, L. Ahlquist, and D.P. Kossives, "Design and characterization of multilayer spiral transmission-line baluns," IEEE Trans. Microw. Theory Tech., vol.47, no.9, pp.1841–1847, Sept. 1999.

[14] S.C. Tseng, C. Meng, C.H. Chang, C.K. Wu, and G.W. Huang, "Monolithic broadband Gilbert micromixer with an integrated Marchand balun using standard silicon IC process," IEEE Trans. Microw. Theory Tech., vol.54, no.12, pp.4362–4371, Dec. 2006.

[15] J.R. Long, "Monolithic transformers for silicon RF IC design," IEEE J. Solid-State Circuits, vol.35, no.9, pp.1368–1381, Sept. 2000.

[16] K.S. Ang and I.D. Robertson, "Analysis and design of impedance-transforming planar Marchand baluns," IEEE Trans. Microw. Theory Tech., vol.49, no.2, pp.402–406, Feb. 2001.

[17] 3GPP TS 36.101 V9.9.0: Technical Specification Group Radio Access Network; Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) radio transmission and reception (Release 9), Dec. 2011.

[18] O. Oliaei, M. Kirschenmann, D. Newman, K. Hausmann, X. Haolu, P. Rakers, M. Rahman, M. Gomez, Y. Chuanzhao, B. Gilsdorf, and K. Sakamoto, "A multiband multimode transmitter without driver amplifier," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp.164–165, San Francisco, CA, Feb. 2012.

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