Digital Correction of Mismatches in Time-Interleaved ADCs for Digital-RF Receivers

Tomoya Takahashi, Takao Kihara, Tsutomu Yoshimura

Osaka Institute of Technology, Japan

December 6, 2017

Outline

Background and Objectives

Mismatch Aliasing Signals

Modeling of TI-ADC in Digital-RF Receivers

Correction Architecture

Complex Mixer and CIC Filter

Mismatch Correction Circuit

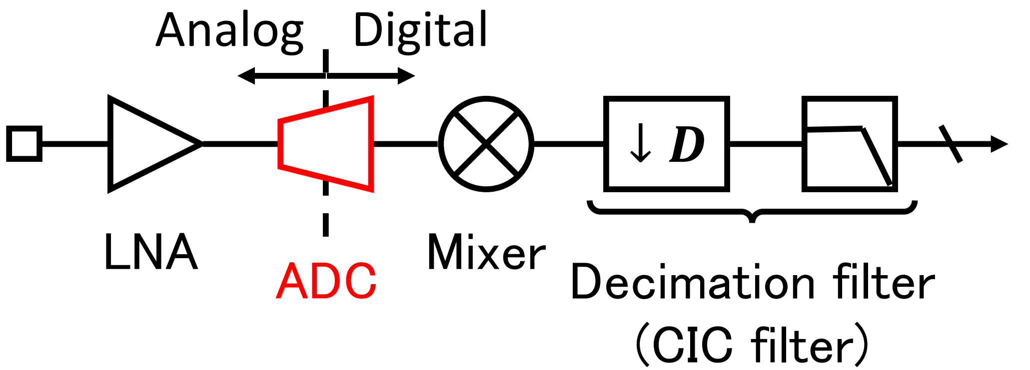
Simulations and Measurements

Summary

Background

Digital-RF Receivers:

- Sample RF signals directly.
- Downconvert and filter the RF signals in digital domain.
- Reduce the design cost and time to market.



LNA: Low-noise amplifier, ADC: Analog-to-digital converter,
CIC: Cascaded integrator-comb, JSSC ’12 [1]

Two requirements for the direct-RF sampling ADC

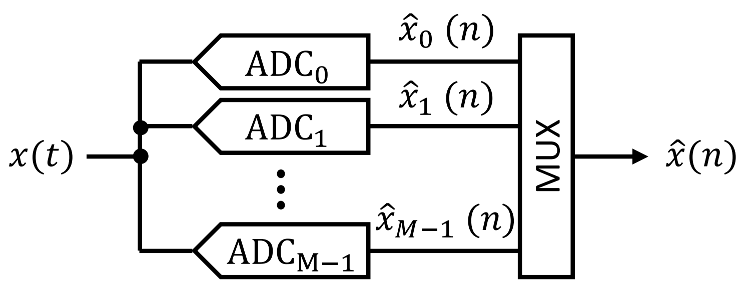
- High-speed sampling (GS/s)
- High SFDR in the desired band (>70 dB)

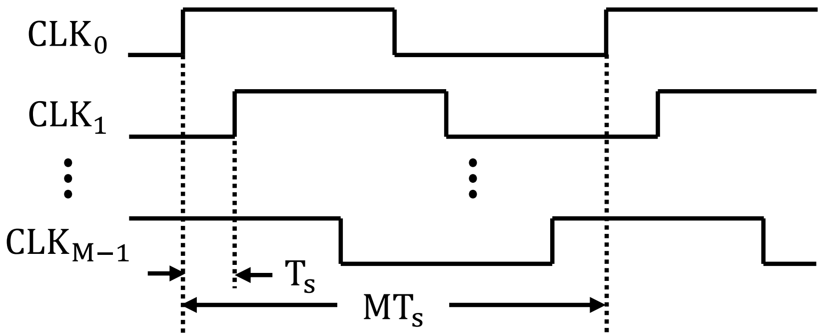
SFDR: Spurious-free dynamic range

Objectives

Time-interleaved ADC (TI-ADC):

- Converts analog signals to digital ones with multiple ADCs.
- Decreases the required sampling rate for one ADC.





Characteristic mismatches among ADCs:

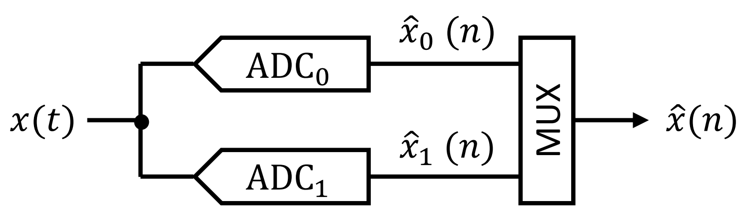
- Generate aliasing signals and degrade the SFDR.
- Must be corrected.

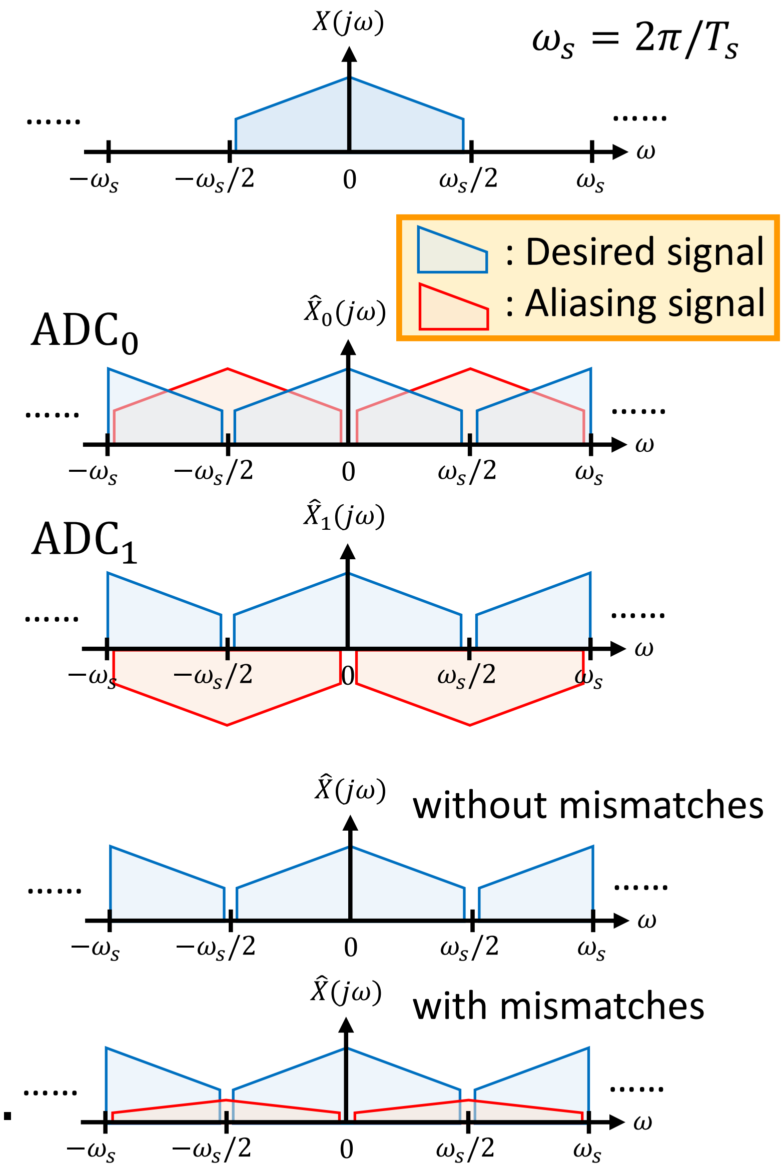
Conventional correction methods (MTT’15[3], TCASI’13[4]) :

- Cannot be applied to digital-RF receivers.
- Become more complex as number of channels increases.

We present a simpler correction method for M-channel TI-ADCs in the receiver.

Modeling of Two-channel TI-ADC





Output spectrum of each ADC

- Desired signal in ADC_0 is in-phase to it in ADC_1.
- Aliasing signals around $\pm\omega_s/2$ in ADC_0 are antiphase to those in ADC_1.

Multiplexing $\hat{x}_0(n)$ and $\hat{x}_1(n)$ cannot completely remove aliasing signals due to mismatches.

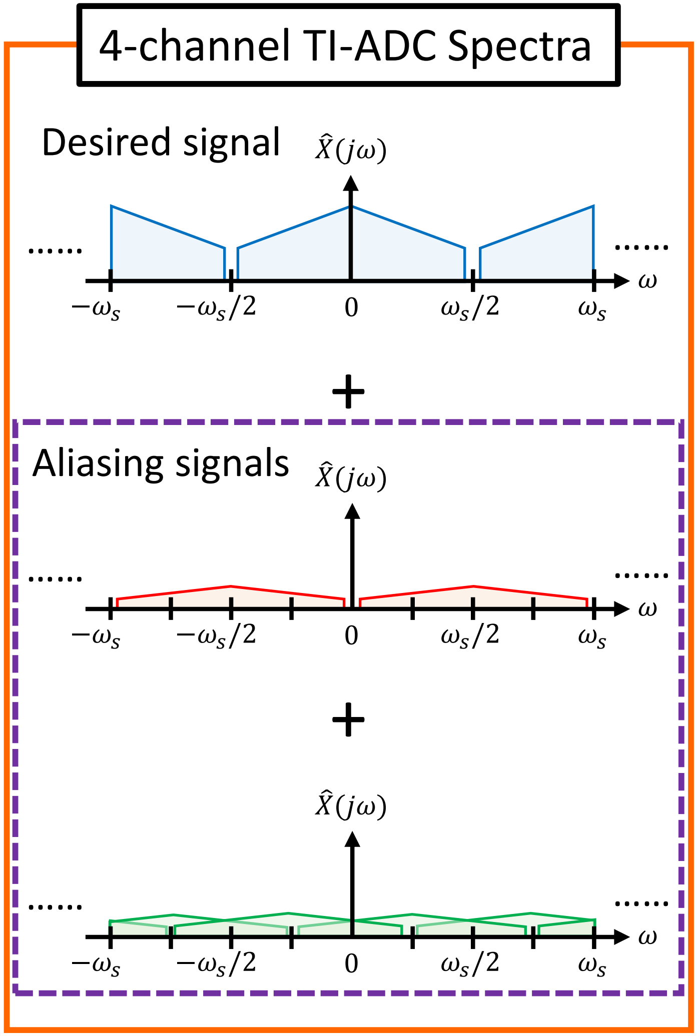
Modeling of M-channel TI-ADC

4-channel TI-ADC

- Aliasing signals appear around $\pm\omega_s l/4$ $(l = 1, 2, 3, \dots)$.

M-channel TI-ADC

- Aliasing signals appear around $\pm\omega_s l/M$ $(l = 1, 2, 3, \dots)$.
- As M increases, more aliasing signals appear.



Correction circuits become more complex as M increases.

Modeling of TI-ADC in Digital-RF Receivers

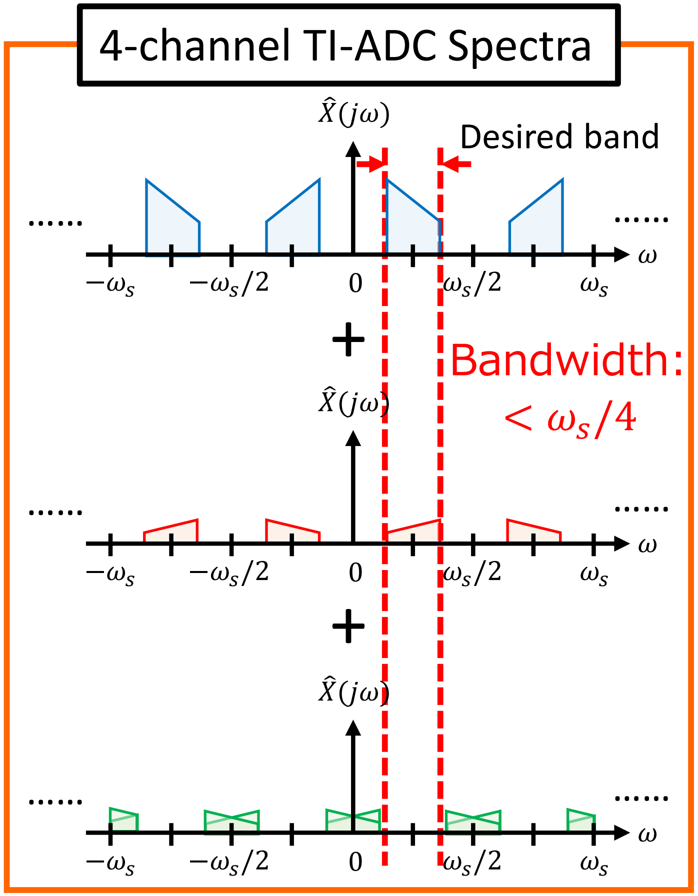
Bandwidth of the RF input signal: $\ll \omega_s$

Conditions

- Bandwidth of input signal: $< \omega_s/M$
- Carrier frequency: $\omega_s/4$

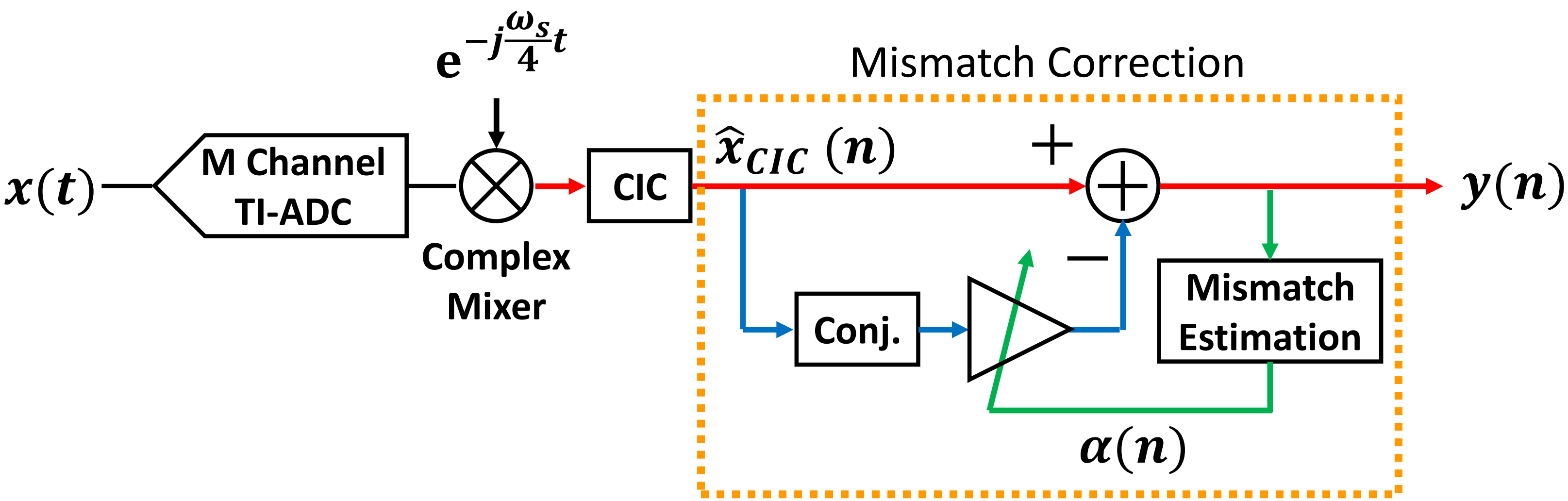
Output spectrum

- In-band (around $\omega_s/4$): one aliasing signal
- Out-of-band: the other aliasing signals



Need to remove only one aliasing signal.

Correction Architecture



Complex mixer and CIC filter:

- Enable the correction block to operate at lower data rates.
- Remove out-of-band aliasing signals.

Simple mismatch correction block:

- Uses complex conjugate of the CIC filter output signal.
- Removes an in-band aliasing signal.

Complex Mixer and CIC Filter

Complex Mixer:

- Multiplies $\hat{x}(n)$ by $\exp(-j\omega_s t/4)$ to downconvert the input signal to the baseband.

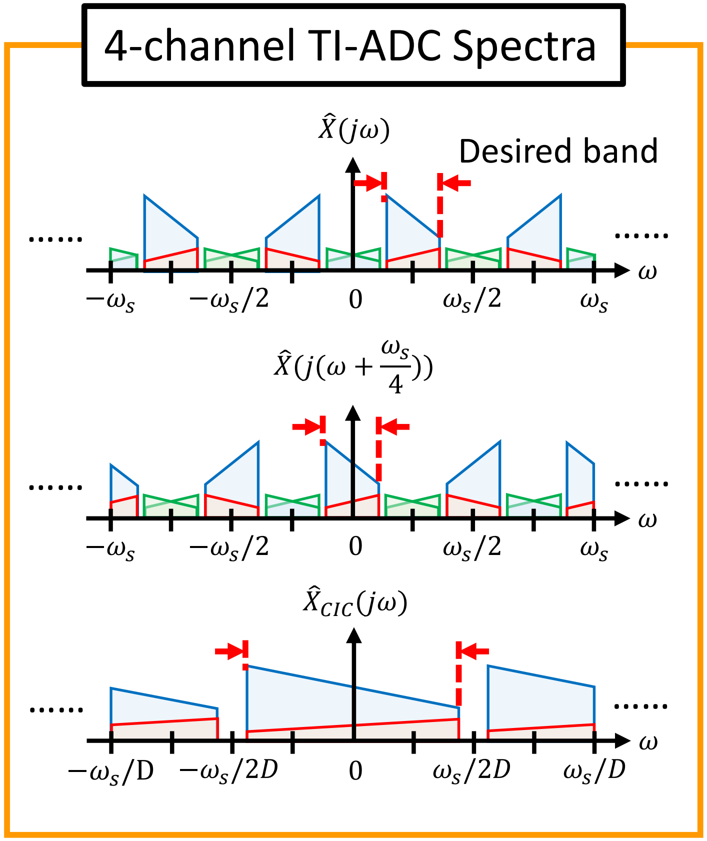
CIC filter:

- Extracts the in-band components.

$$H_{CIC}(z) = \left(\frac{1}{D} \cdot \frac{1 - z^{-D}}{1 - z^{-1}}\right)^L$$

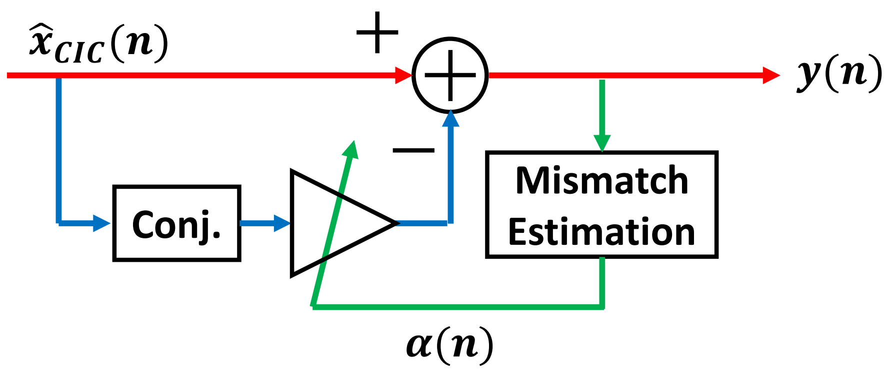
D: Number of decimation
L: Order of the filter

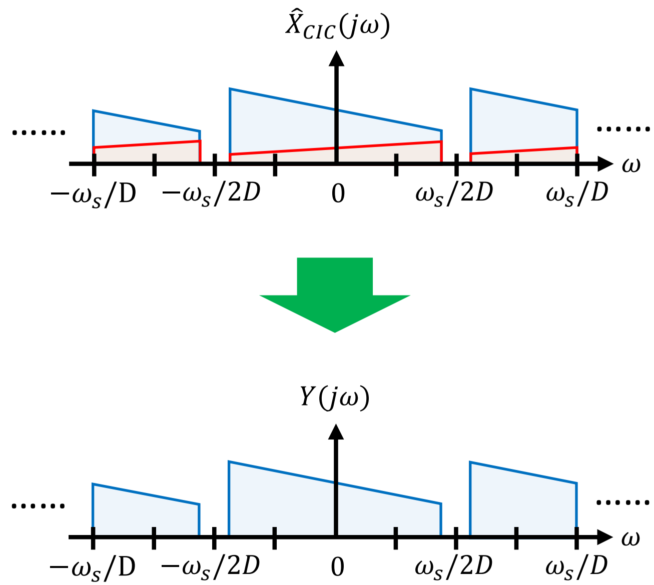
- Removes the aliasing signals around $\pm\omega_s l/M$ by setting D to M.



The decimated signal has only in-band components.

Mismatch Correction





Correction signal, $\alpha(n)\hat{x}^*_{CIC}(n)$

- Multiplying complex conjugate of $\hat{x}_{CIC}(n)$ by $\alpha(n)$.

Correction coefficient, $\alpha(n)$

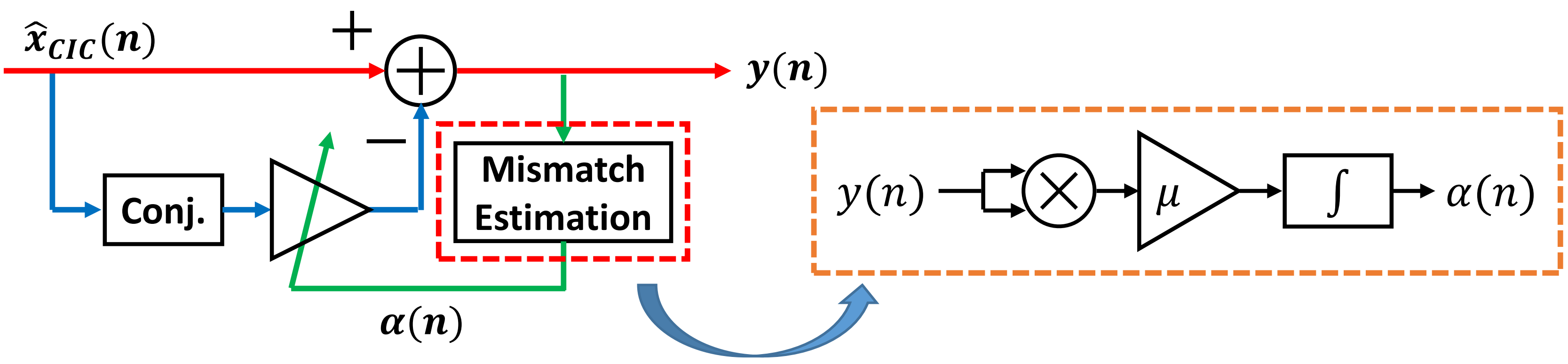
- Generated by mismatch estimation block.

Corrected signal, $y(n)$

- Subtracting the correction signal from $\hat{x}_{CIC}(n)$.

$$y(n) = \hat{x}_{CIC}(n) - \alpha(n)\hat{x}^*_{CIC}(n)$$

Mismatch Estimation



Detects the complex conjugate of $y(n)$ with CACF

- No mismatches: $C_y(0) = E[y^2(n)] = E\left[y(n)\left(y^*(n)\right)^*\right] = 0$

CACF: Complementary auto-correlation function,
$E[\ ]$: Expected value

Adaptive signal processing:

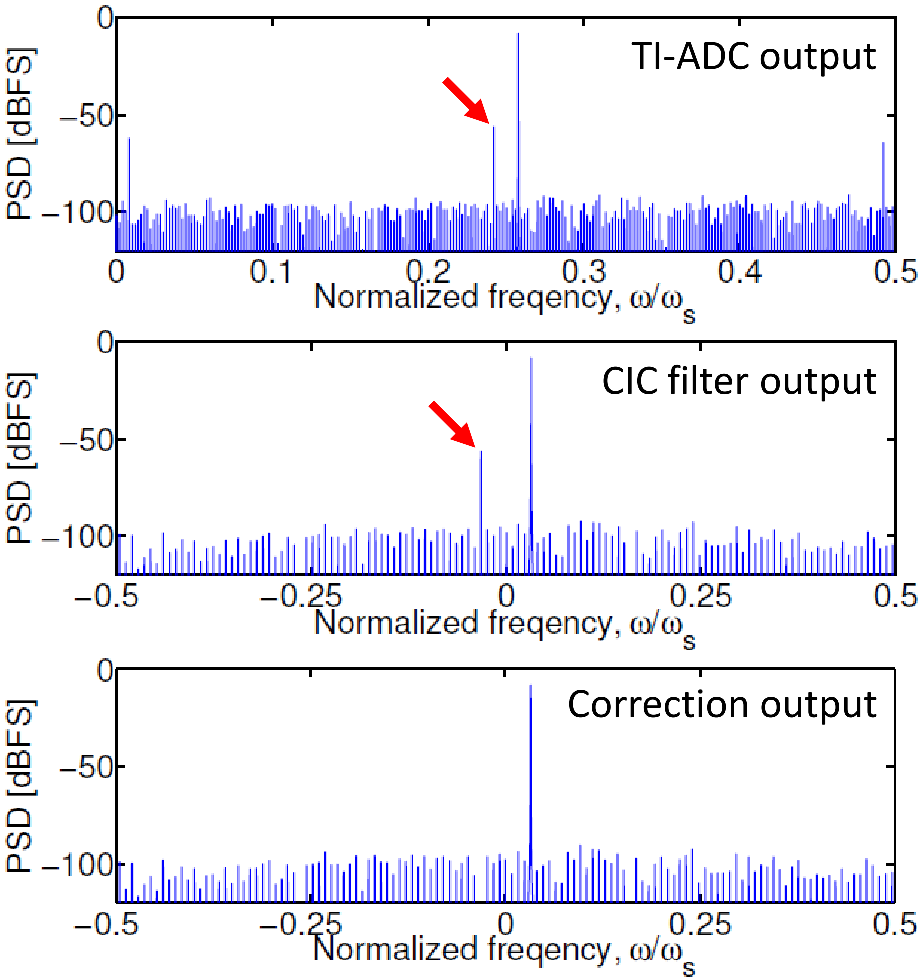
- Allows $C_y(0)$ to be zero to remove the aliasing signals.

$$\alpha(n+1) = \alpha(n) + \mu y^2(n)$$

μ: Adaptive step size

Simulated Spectra

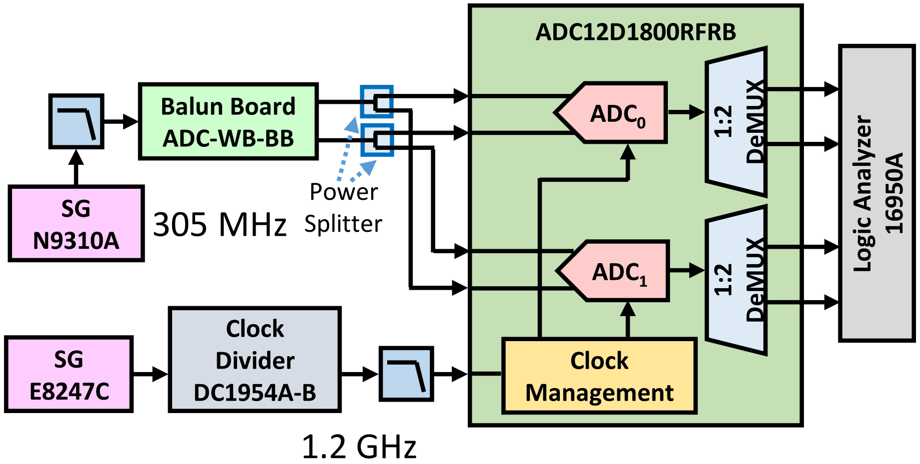
Simulations of a 4-channel 12-bit TI-ADC

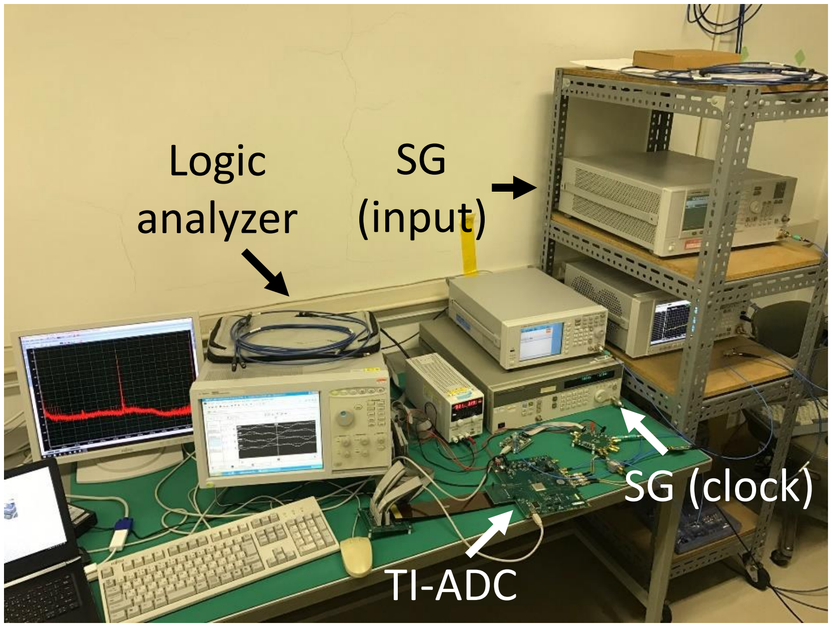


Simulation conditions	
Samples	2^{14}
CIC filter	$D = 4$
	$L = 2$
Input signal	$\omega_{in} = 0.258\omega_s$
	$P_{in} = -8$ dBFS
Gain mismatch of each channel	$0, -2^{-10}, -2^{-11}, -2^{-9}$
Sampling-Time mismatch of each channel	$0, -2^{-7}, -2^{-9}, -2^{-8}$
Adaptive step size	2^{-36}

A -50 dBFS aliasing signal was reduced to the noise floor.

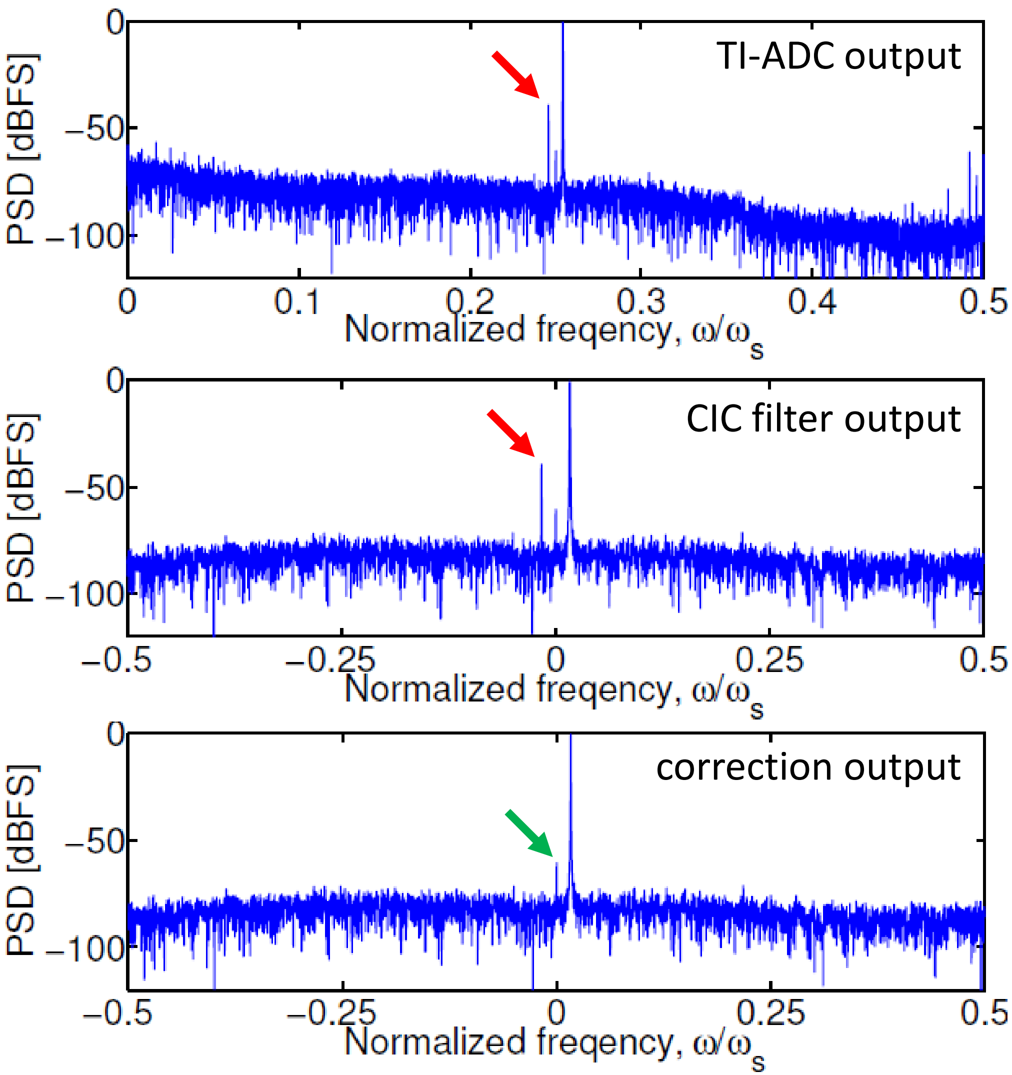
Measurement Setup





- A commercial 2-channel 12-bit TI-ADC was used.
- The frequencies of the sampling clock and input signal were 1.2 GHz and 305 MHz.
- The digital output signal was acquired with a logic analyzer and corrected by using an FPGA.

Measured Spectra



Measurement conditions	
Samples	2^{14}
CIC filter	$D = 4$
	$L = 2$
Input signal	$f_{in} = 305$ MHz
	$P_{in} = -0.5$ dBFS
Adaptive step size	2^{-36}

A -40 dBFS aliasing signal was reduced to the noise floor.

Comparison

	Number of ADC channels	Bandwidth	Number of adders	Number of multipliers	FIR filters
This work	M	$\pm\omega_s/2M$	7	7	No
MTT'15 [3]	2	$\pm\omega_s/2$	6 or 8	7	HTF
TCAS-I'15 [6]	4	$\pm\omega_s/2$	27	21	HTF, LPF, HPF
TCAS-I'13 [4]	M	$\pm\omega_s/2$	$2M-1$	$4(M-1)$	Derivative filter

HTF: Hilbert transform filter, LPF: Low-pass filter, HPF: High-pass filter

The proposed method needs

- The minimum number of adders and multipliers ($M \geq 4$)
- No FIR filters

Summary

Presented a mismatch correction method employing the downconverted and decimated signals:

- ➢Enables the correction block to operate at lower data rates
- ➢Removes out-of-band aliasing signals

The aliasing signals are reduced on:

- ➢Simulations of a 4-channel 12-bit TI-ADC
- ➢Measurements of a 2-channel 12-bit TI-ADC

The proposed method can be implemented more simply and completely remove the aliasing signals.

FPGA

Logic resources	Used	Total	Percentage used
ALM	103	18480	0.6 %
DSP block	10	66	15.2 %

This table summarizes the logic resources of the proposed mismatch correction circuit on the FPGA.

Convergence behaver of coefficient α