A Polyphase Decimation Filter for Time-Interleaved ADCs in Direct-RF Sampling Receivers

Yuma Isobe, Takao Kihara, Tsutomu Yoshimura

Osaka Institute of Technology, Japan

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Outline

Background and objectives

Decimation filter for Conventional direct-RF sampling receiver with
N-channel time-interleaved ADC (TI-ADC)

Proposed direct-RF sampling receiver

Polyphase decimation filter with a decimation factor twice as large as *N* ($D = 2 \times N$)

Simulations and comparisons

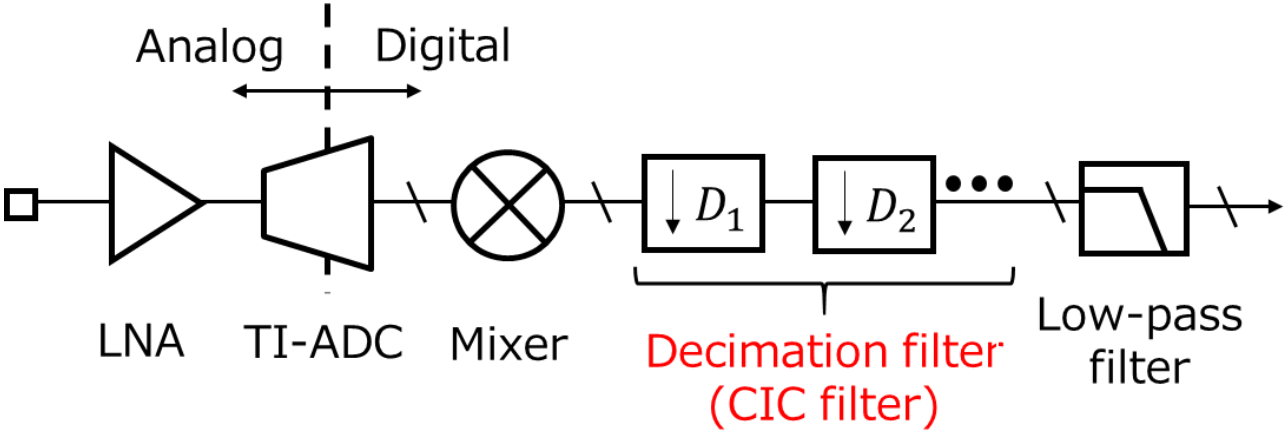
Output spectrum
Power consumption
Chip area

Summary

Background

Direct-RF sampling receiver

- Downconverts and filters the RF signals in digital domain.
- Benefits from technology scaling and design automation.
- Reduces the design cost and time to market.



LNA: Low-noise amplifier, ADC: Analog-to-digital converter,
CIC: Cascaded integrator-comb, D: Decimation factor

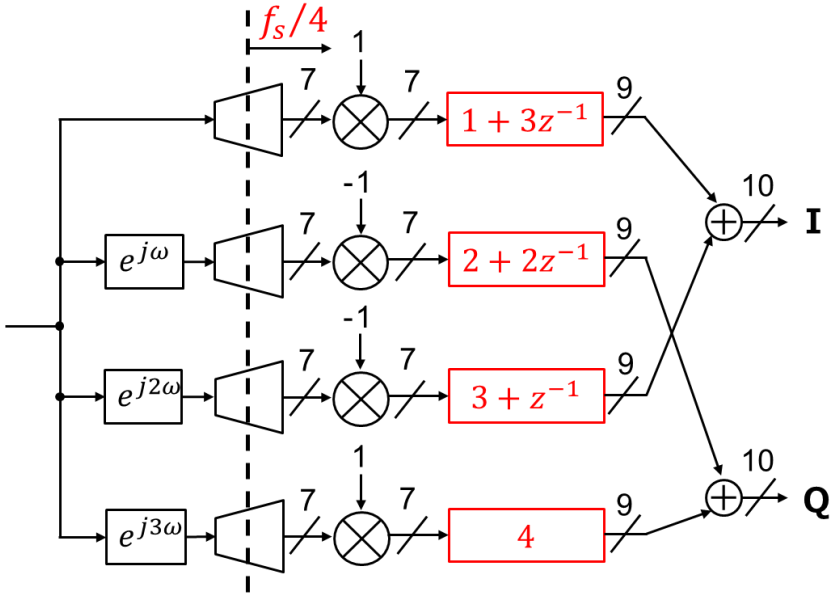
Decimation filter

- Decreases high data rates (>3 GS/s) to low ones (MS/s).
- Reduces the quantization noise of the ADC.

Objectives

Conventional decimation filter (E.Martens, *et al.*, JSSC 2012)

- Decimation factor, D = Channel number of TI-ADC, N
- Adders need to work at 1 GS/s for 4-GS/s 4-channel TI-ADC.
- Difficulty in realizing medium-bit (6-10) additions for 1 GS/s.

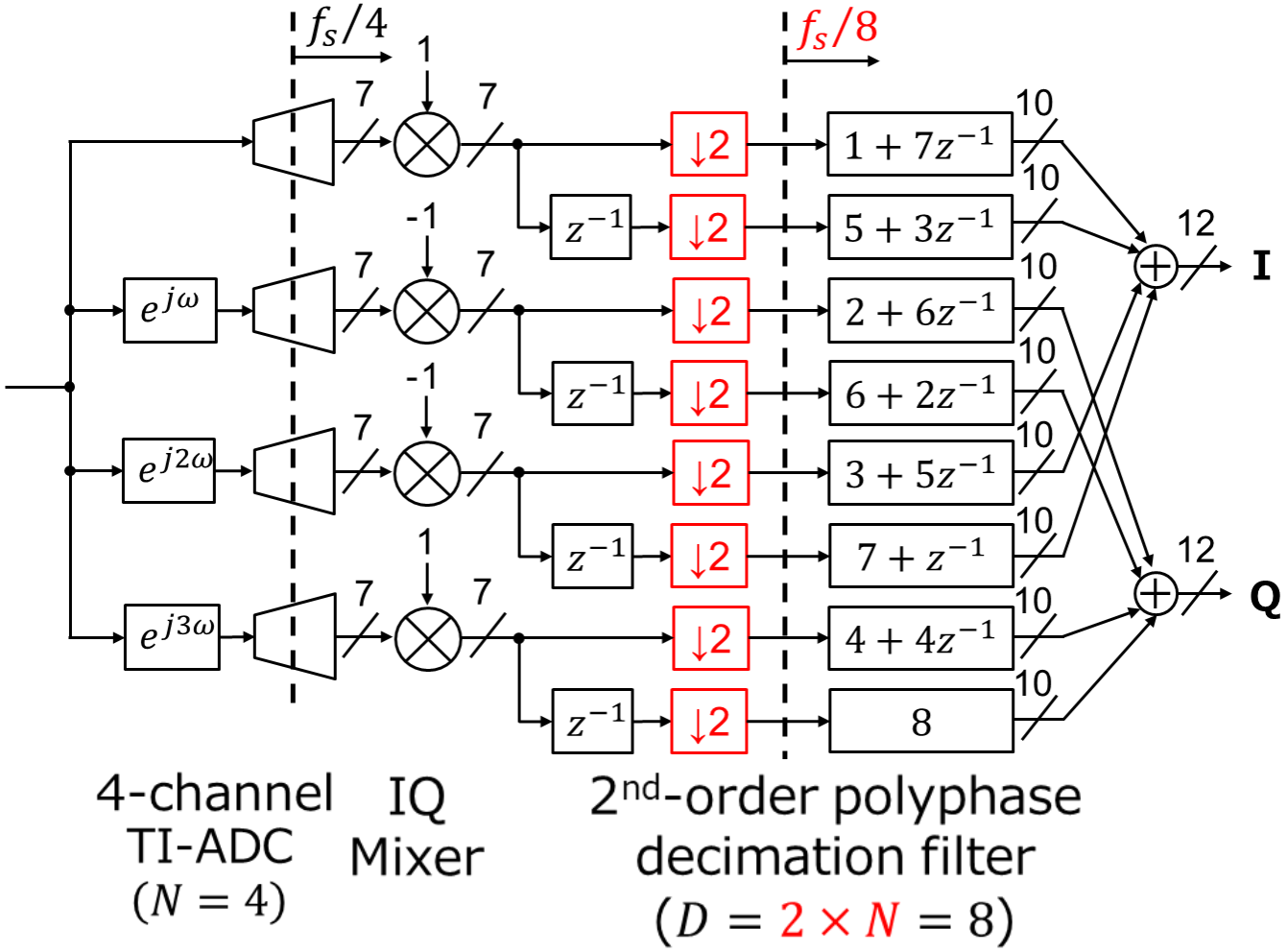


4-channel TI-ADC ($N = 4$) | IQ mixer | 2nd-order polyphase decimation filter ($D = N = 4$)

f_s: Sampling frequency
I/Q mixer: In-phase/quadraturephase downconversion mixer

We present a polyphase decimation filter to relax the speed requirement of the adders.

Proposed Polyphase Filter for 4-Channel TI-ADC



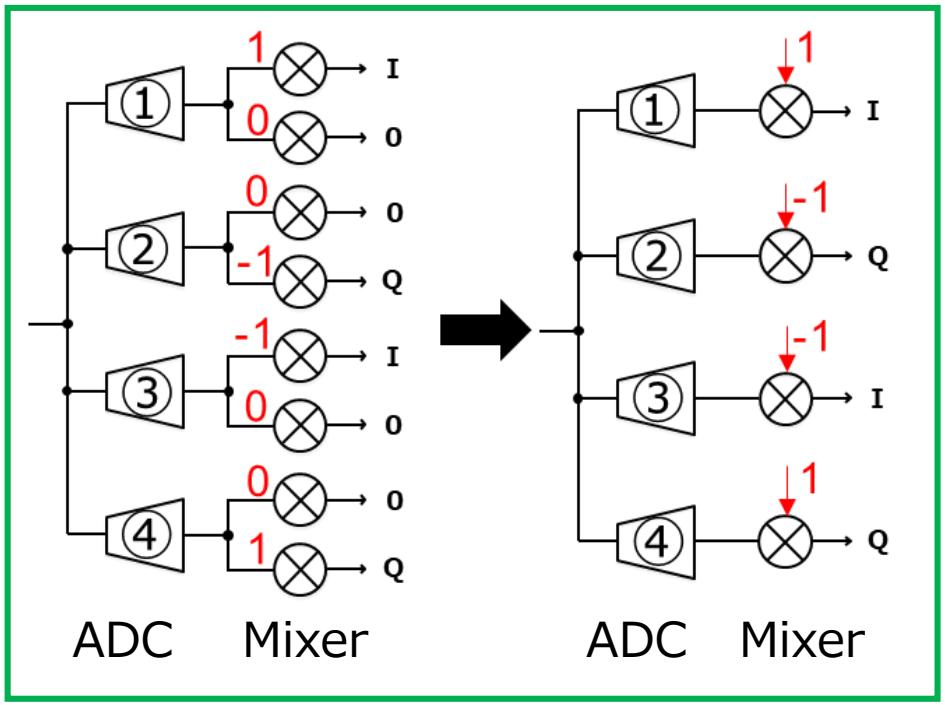
- $D = 2 \times N (= 8)$
- Adders work at 500 MS/s for 4-GS/s 4-channel TI-ADC.

We can realize higher-speed decimation filter with little additional power consumption and chip area.

I/Q Mixer

- Downconverters the digitized signal to baseband with a complex signal, $exp(-j(2\pi f_s/4)t)$.

$$e^{-j\left(2\pi\frac{f_S}{4}\right)t}\Big|t = nT_s$$
$$= \underbrace{\cos\left(\frac{\pi}{2}n\right)}_{[1,0,-1,0]} - \underbrace{j\sin\left(\frac{\pi}{2}n\right)}_{[0,-1,0,1]}$$



- Eliminate all mixers using 0 and realize I/Q mixing only with multiplications of 1 and -1.

This greatly reduces the hardware cost.

Polyphase Decimation Filter

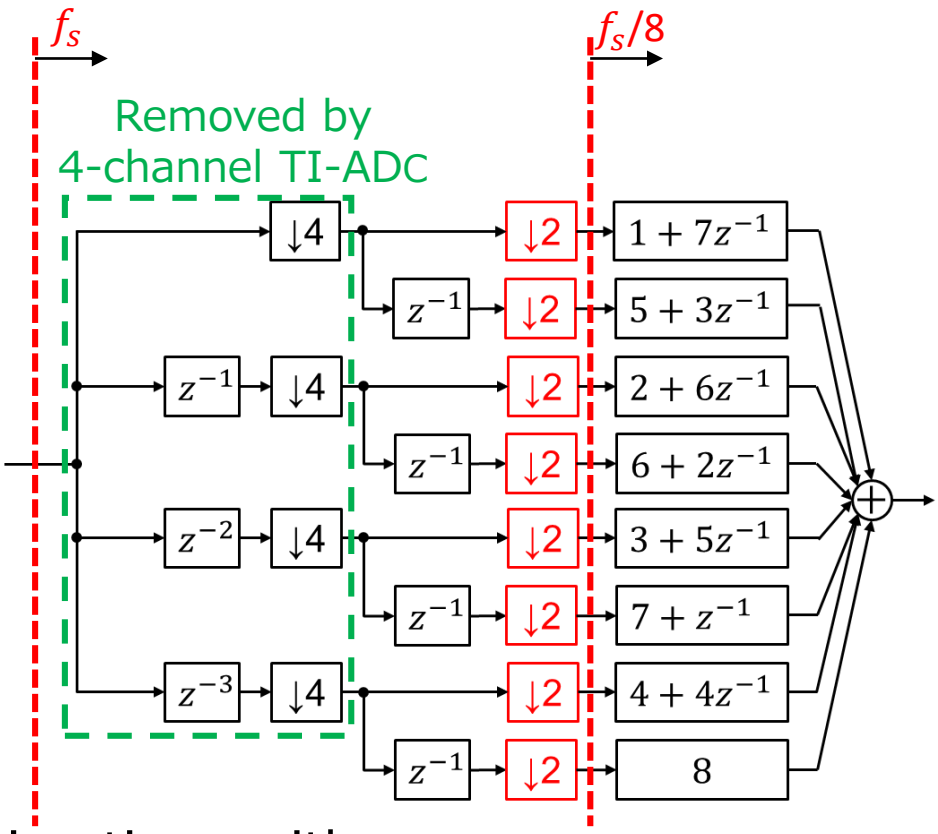
2nd-order CIC filter with $D = 8$

- Transfer function

$$H_{CIC}(z) = \left(\frac{1}{8} \cdot \frac{1 - z^{-8}}{1 - z^{-1}}\right)^2$$

- Polyphase decomposition

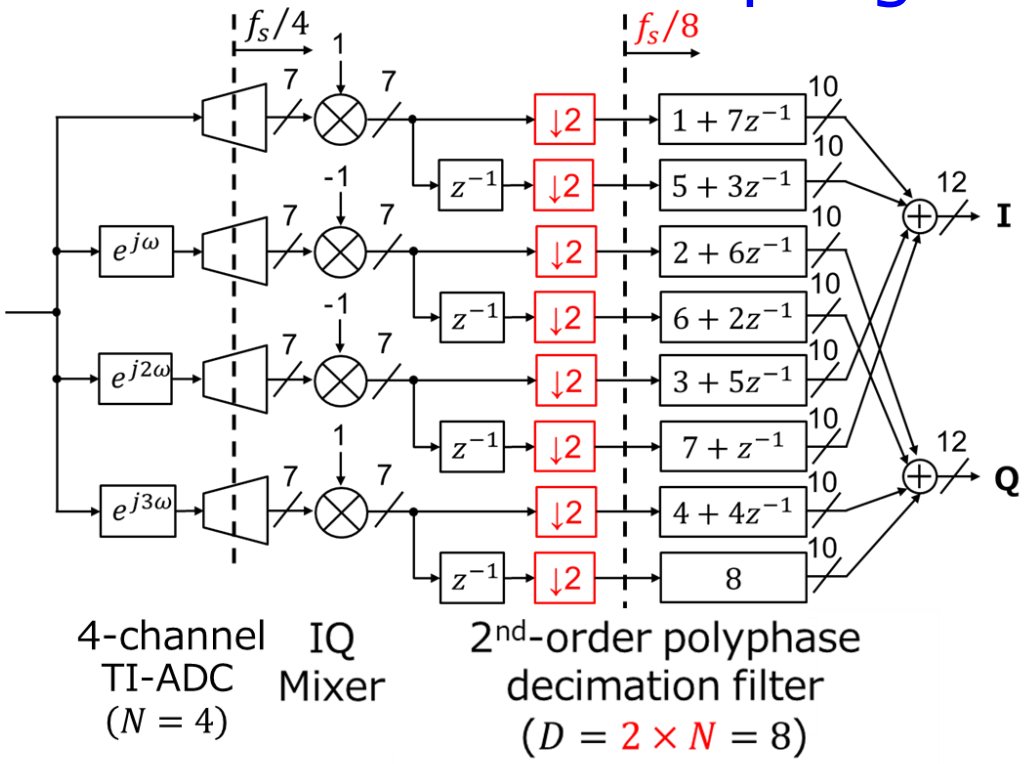
$$H_{CIC}(z) =$$
$$\frac{1}{8}[(1 + 7z^{-8}) + z^{-4}(5 + 3z^{-8})$$
$$+z^{-1}\{(2 + 6z^{-8}) + z^{-4}(6 + 2z^{-8})\}$$
$$+z^{-2}\{(3 + 5z^{-8}) + z^{-4}(7 + z^{-8})\}$$
$$+z^{-3}\{(4 + 4z^{-8}) + 8z^{-4}\}]$$



- First three delays and four decimations with $D = 4$ can be removed in a 4-channel TI-ADC.

Decimators with D=2 are inserted before the adders, reducing the operating speeds to $f_s/8$.

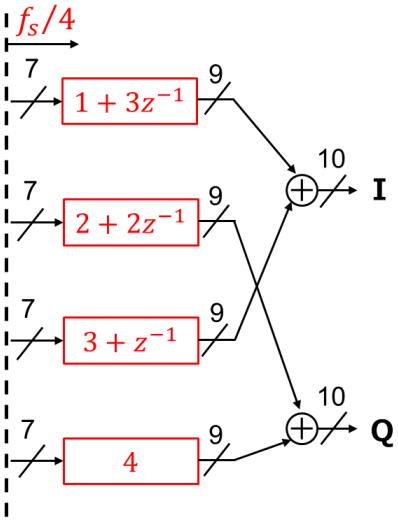
Simulations of Direct-RF Sampling Receiver



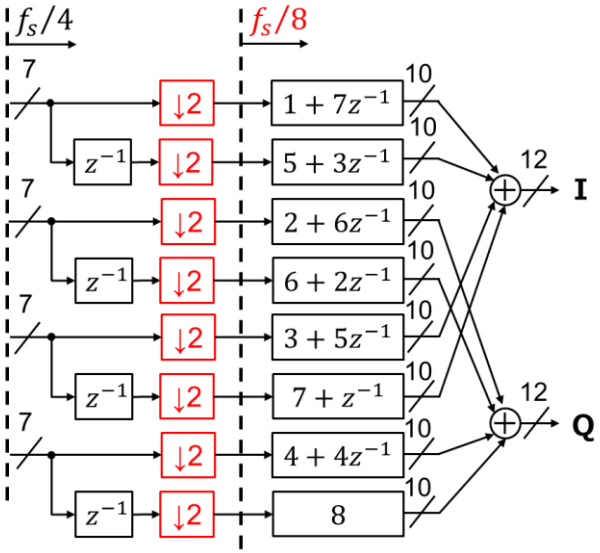
- Process: Renesas 65 nm SOTB CMOS
- HDL: Verilog HDL
- Perfomances: Output spectum, chip area, power consumption
- Tools: Mathworks MATLAB/Simulink, Candence Verilog-XL, Synopsys Design Compiler, IC Compiler

SOTB: Silicon on thin buried oxide

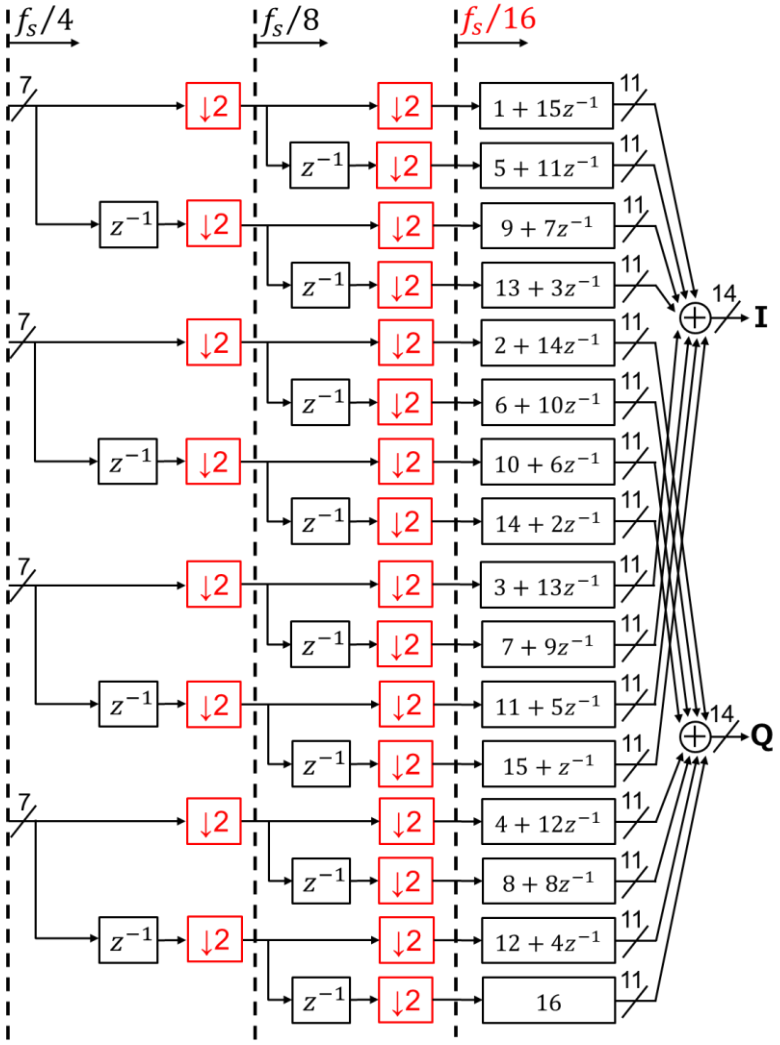
Comparison of Polyphase Decimation Filters



$D = N = 4$ (conventional)

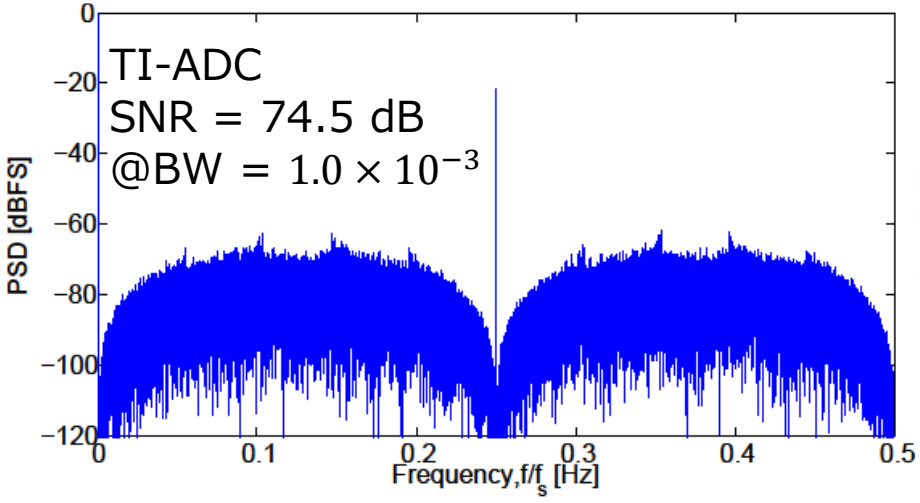


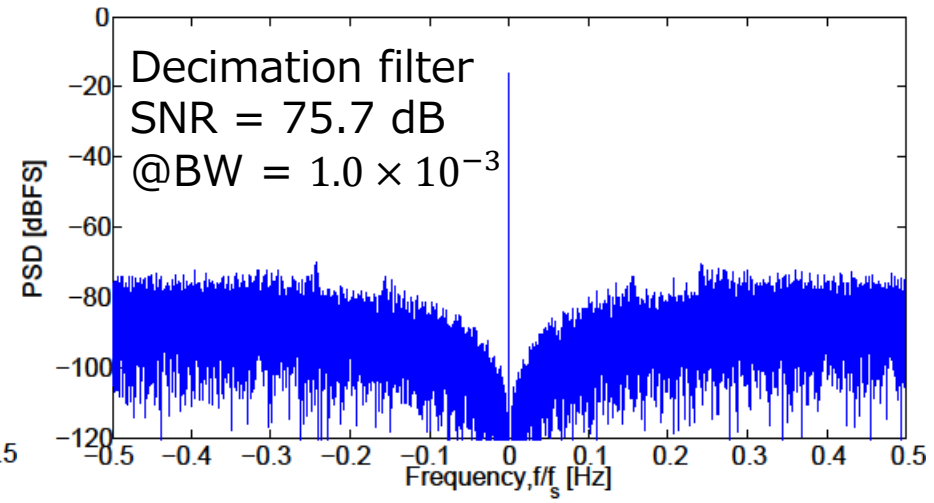
$D = 2 \times N = 8$ (proposed)



$D = 4 \times N = 16$ (comparative)

Output Spectrum (Proposed)





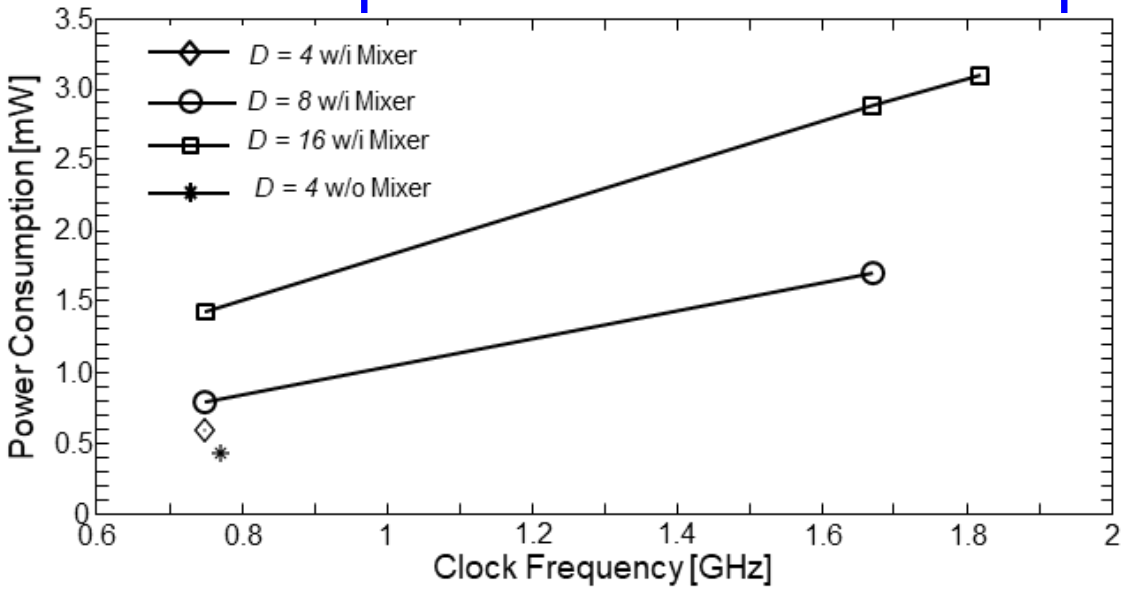
Simulation conditions on MATLAB/Simulnk	
Number of data: N_D	$2^{18}(= 262{,}144)$
Sampling frequency: f_s	1
Frequency of input signal: f_{in}	$f_s/4 + 4/N_D$
Amplitude of input signal: A_{in}	0.2

BW:Bandwidth

- Desired signal was downconverted around DC.
- Output SNR did not change.

The filter combined with the mixers works properly.

Power Consumption vs. Clock Frequency



➢Conventional filter (D = 4)

・Lowest power consumption at 0.77 GHz.

・Cannot operate at more than 0.77 GHz due to the adders.

➢Proposed filter (D = 8)

・Operates at 1.67 GHz.

・More power consumption than D =4.

➢Comparative filter (D = 16)

・Works at 1.82 GHz, limited by D-flip flops.

・Most power consumption.

Conditions

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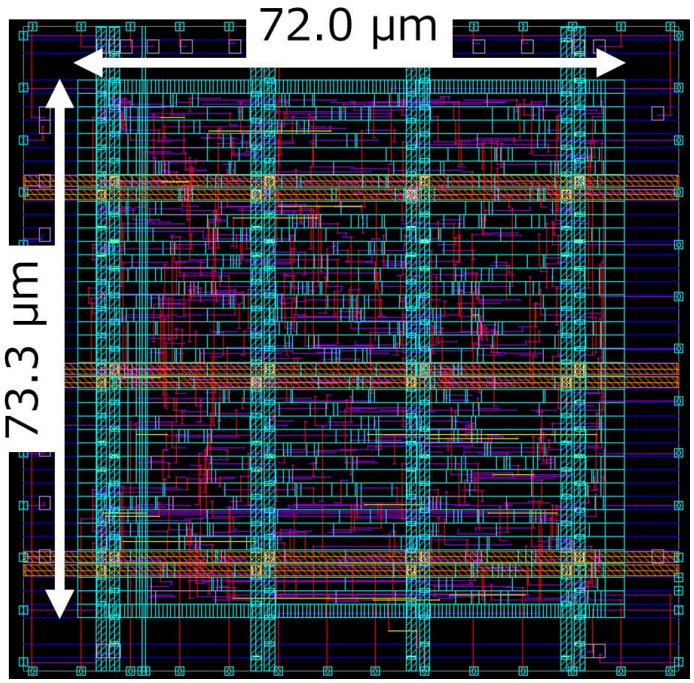
V_{DD} = 0.75 V, B_{in} = 7

V_{DD}: Supply voltage

B_{in}: Input bit width

Layout and Chip Area (Proposed)



Proposed filter
(D = 8) with I/Q mixers

D	Chip area $[\mu m^2]$	
	w/i I/Q Mixer	w/o I/Q Mixer
4 (conventional)	2791	2000
8 (proposed)	5280	5205
16	13057	13001

(From Synopsys IC Compiler)

The proposed filter consumes twice or more chip area of the conventional one.

Summary

Polyphase decimation filter with $D = 2 \times N$ for N-channel TI-ADCs in direct-RF sampling receivers

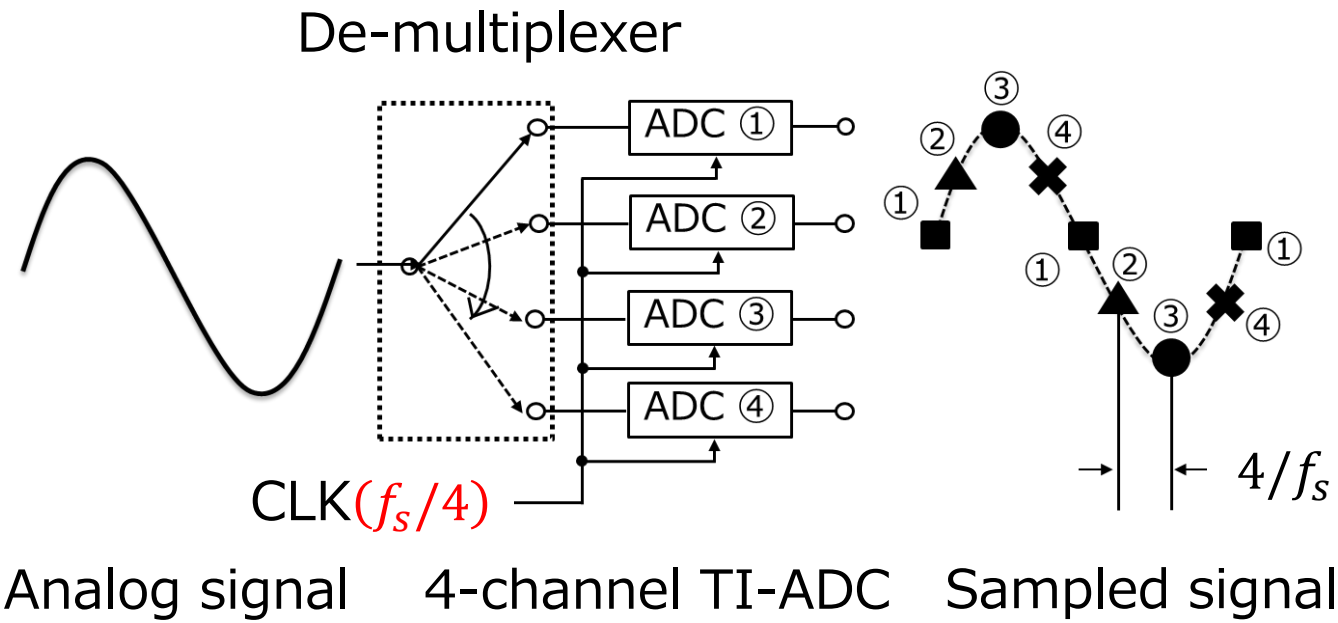
- Decimators with $D = 2$, inserted before adders, enable the filter to operate at twice the operating frequency of the conventional method ($D = N$).
- A 7-bit polyphase decimation filter with $D = 8$ and I/Q mixers are designed in a 65-nm SOTB CMOS process.
- Simulations show that the proposed filter works properly at 1.67 GHz with 1.7 mW.

Time-Interleaved ADC (TI-ADC)

4-channel TI-ADC

- Converts analog signals to digital ones with four ADCs.
- Decreases the required sampling rate for one ADC to $f_s/4$.

- The sampled signals are multiplexed together to generate a signal sampled at f_s.
- This multiplexer can be realized by the addition in the decimation filter.



Polyphase Decimation Filter with 4-channel TI-ADC (2nd-order CIC filter with D = 16)

- The transfer function:

$$H_{CIC}(z) = \left(\frac{1}{16} \cdot \frac{1 - z^{-16}}{1 - z^{-1}}\right)^2$$

Polyphase decimation filter can be obtained by polyphase decomposition of the transfer function.

First three delays and four decimations with D=4 can be removed in a 4-channel TI-ADC.

- This Filter is used comparative architecture.

Reducing the operating speeds of the adders to $f_s/16$.