A Standard-cell Based A/D Converter with a Back-gate VCO and a Fat Tree Encoder

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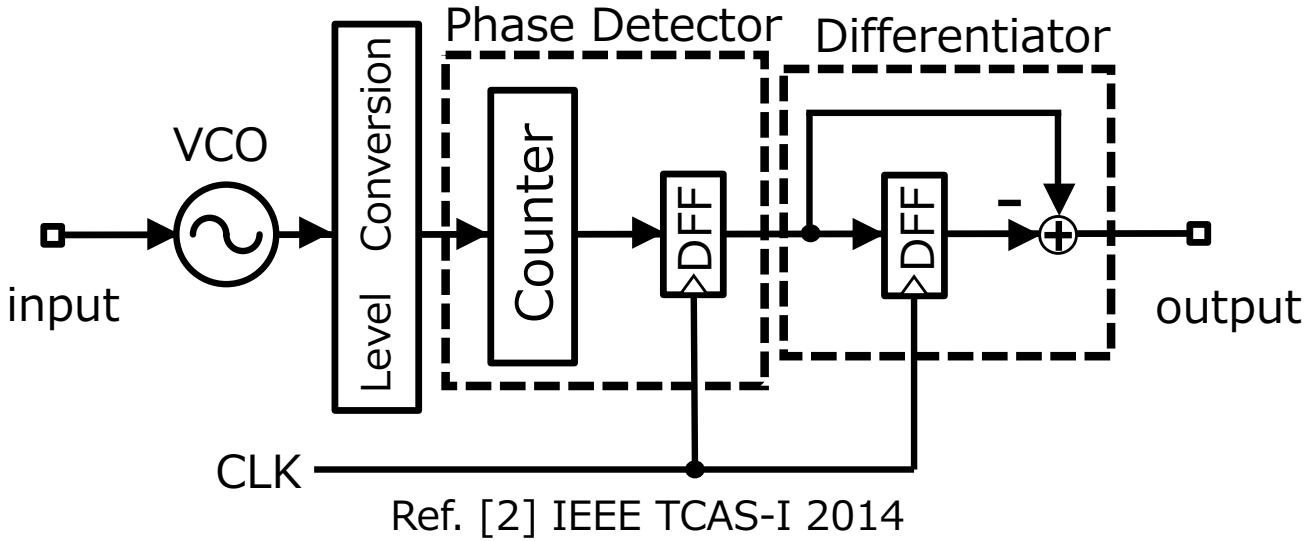
Outline

- Background and objectives
- Proposed VCO-based A/D converter (ADC) with standard cells
  - Back-gate voltage-controlled oscillator (VCO)
  - Sampler
  - Phase detector using fat tree encoder
- Simulation and comparison
- Summary

Background

- VCO-based ADC
  - Consists of only digital standard cells ⇒ Low cost and faster time to market
  - Achives noise shaping ⇒ High signal-to-noise-ratio (SNR)

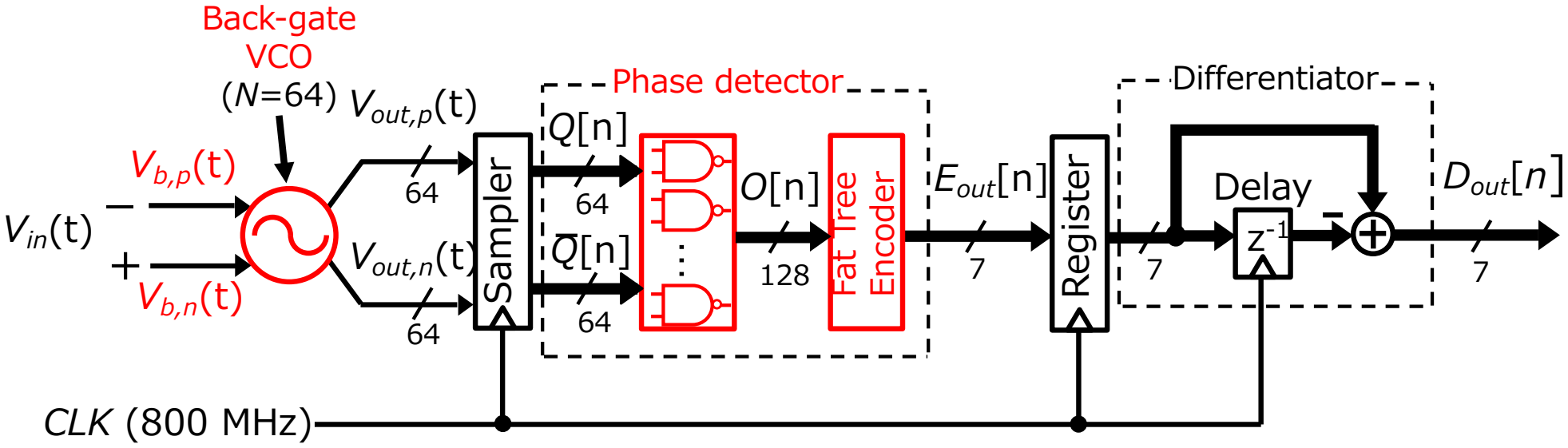


Ref. [2] IEEE TCAS-I 2014

- Conventional VCO-based ADC
  - Changes the oscillation frequency with the supply voltage.
  - Level conversion keeps the output amplitude constant, increasing power consumption.
  - Counter detecting the phase of VCO signal is not suitable for high-speed sampling due to adders (200 MS/s).

Objectives

- Proposed VCO-based ADC

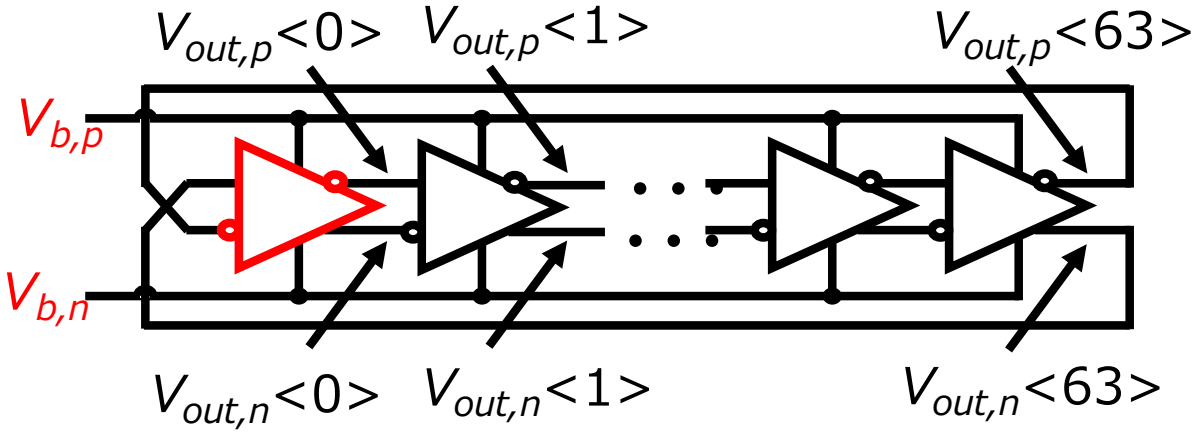


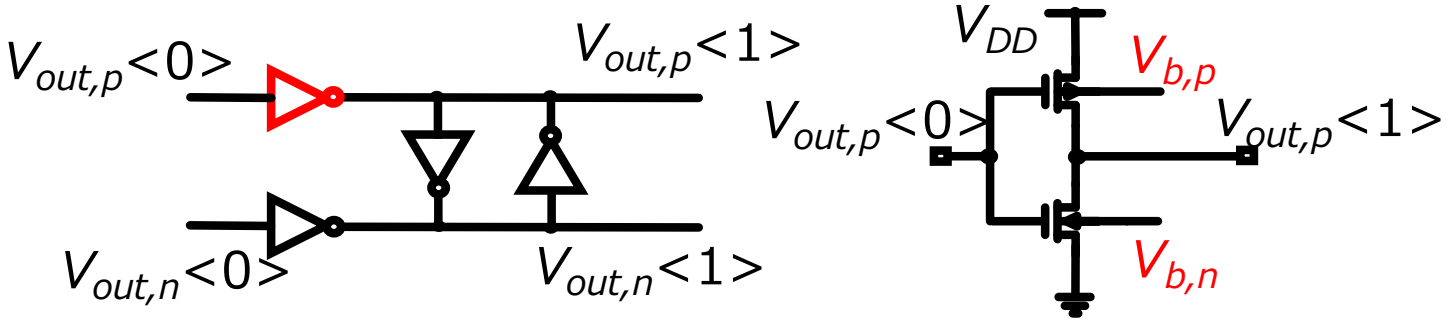
- Back-gate VCO
  - Keeps its output amplitude constant without level conversion.

- Phase detector using fat tree encoder
  - Can operate at higher sampling frequencies (800 MS/s), increasing SNR.

We show the effectiveness of the proposed ADC by simulation.

Back-Gate VCO

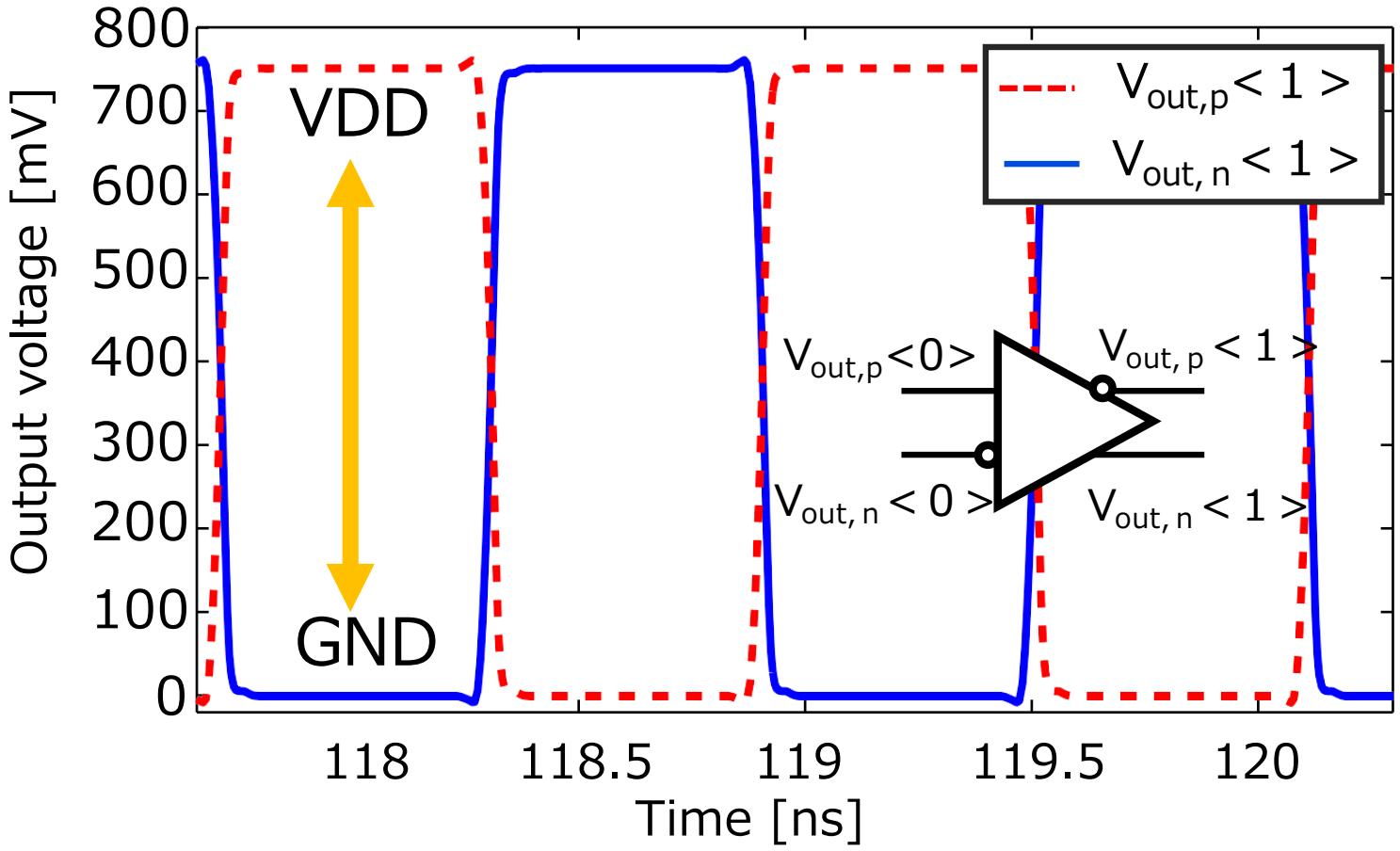




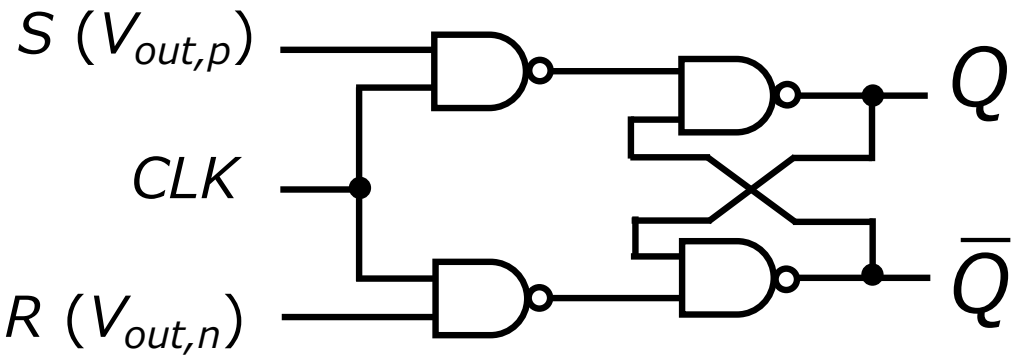
- Ring VCO consists of 64 pseudo-differential delay cells.
- Differential input ($V_{b,n}$-$V_{b,p}$) increases the SNR of the ADC.
- Delay cells consist of NOT gates.
- Oscillation frequency is controlled by the back-gate voltages ($V_{b,p}$, $V_{b,n}$).
- Generates rail-to-rail (GND–VDD) oscillation signals, because the inverter inherently has a rail-to-rail swing and the back-gate control needs no voltage headroom.

Output Signals of Back-Gate VCO

- Back-gate VCO simulated with Cadence Specter RF
  - Input voltage : 0 ~ 750 mV (V_{DD}).
  - Output signals : 0 ~ 750 mV
  - The output signals Can be sampled by digital latchs without the level conversion.
  - Oscillation frequency : 184 MHz ~ 318 MHz (VCO gain, K_{vco} = 89.3 MHz/V)



Sampler (Set/Reset Latch)



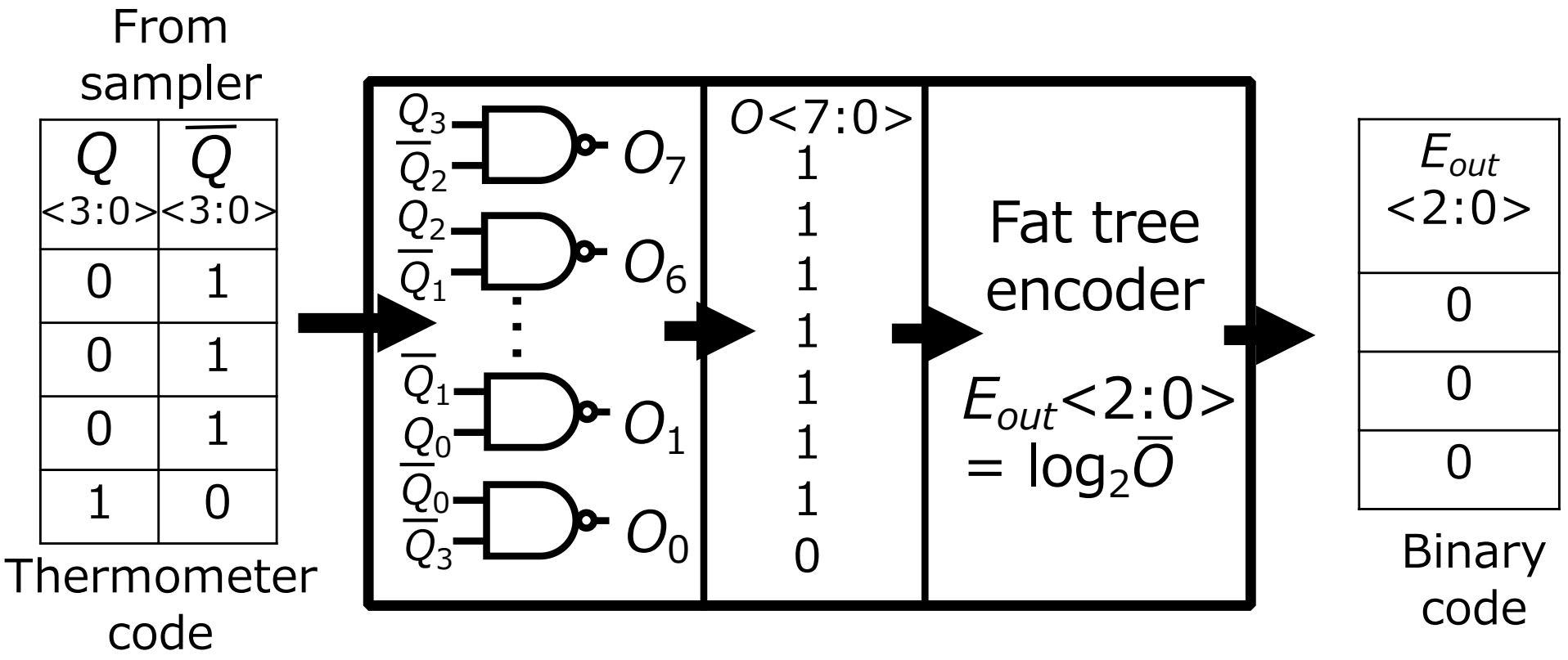
CLK	*S*	*R*	*Q*
0	×	×	Hold
1	1	0	1
1	0	1	0

- Consists of NAND gates.
- Activated by the high level of CLK with a period of *Ts*(=1/*fs*), And then, it quantizes the difference between $V_{out,p}$ and $V_{out,n}$ without differential DFFs.

fs: Sampling frequency, DFF: D-flip flop

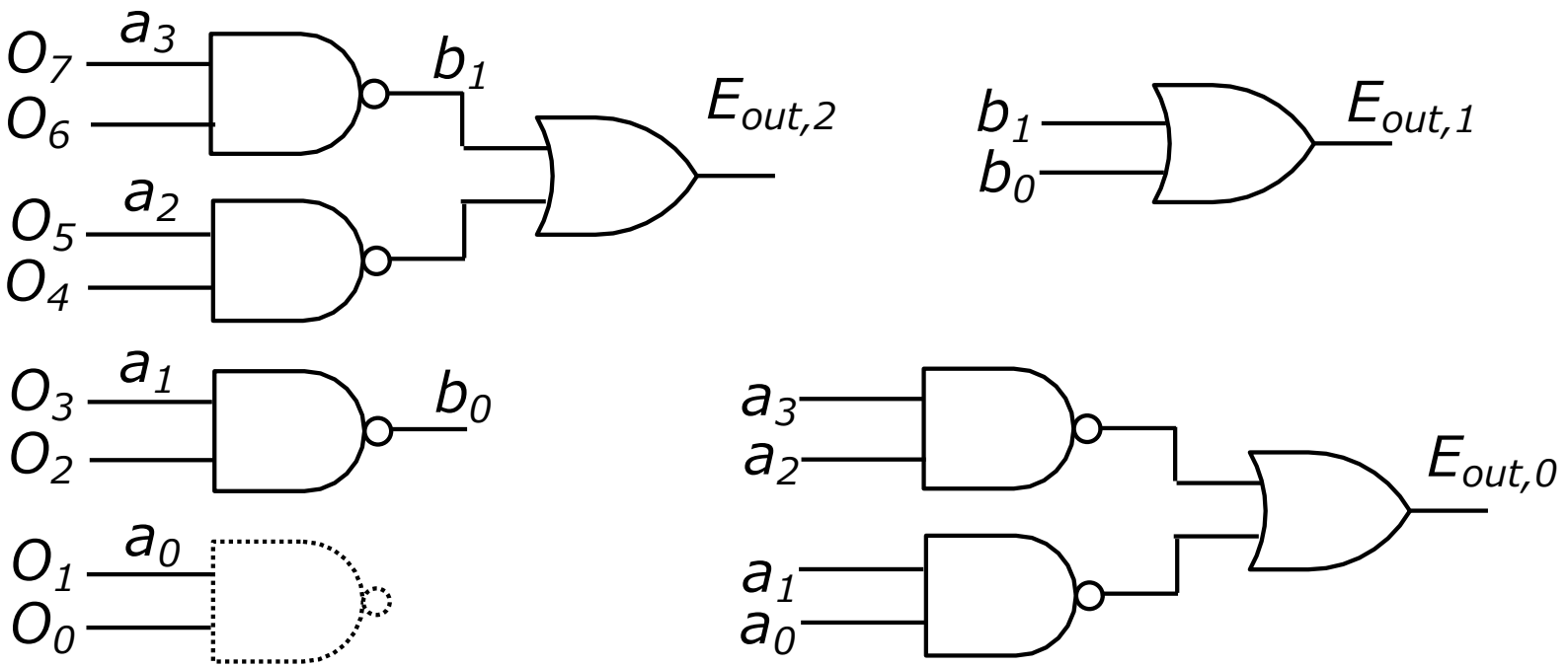
Phase Detector (4-Stage Ring VCO)

- Finds where the outputs of the ring VCO invert and produces the position in a binary code.



1. NAND gates output a sequence consisting of many 1s and one 0, representing the boundary between 0 and 1 of *Q*.
2. Fat tree encoder outputs the bit position of 0 in a binary code.

Fat Tree Encoder (4-Stage Ring VCO)



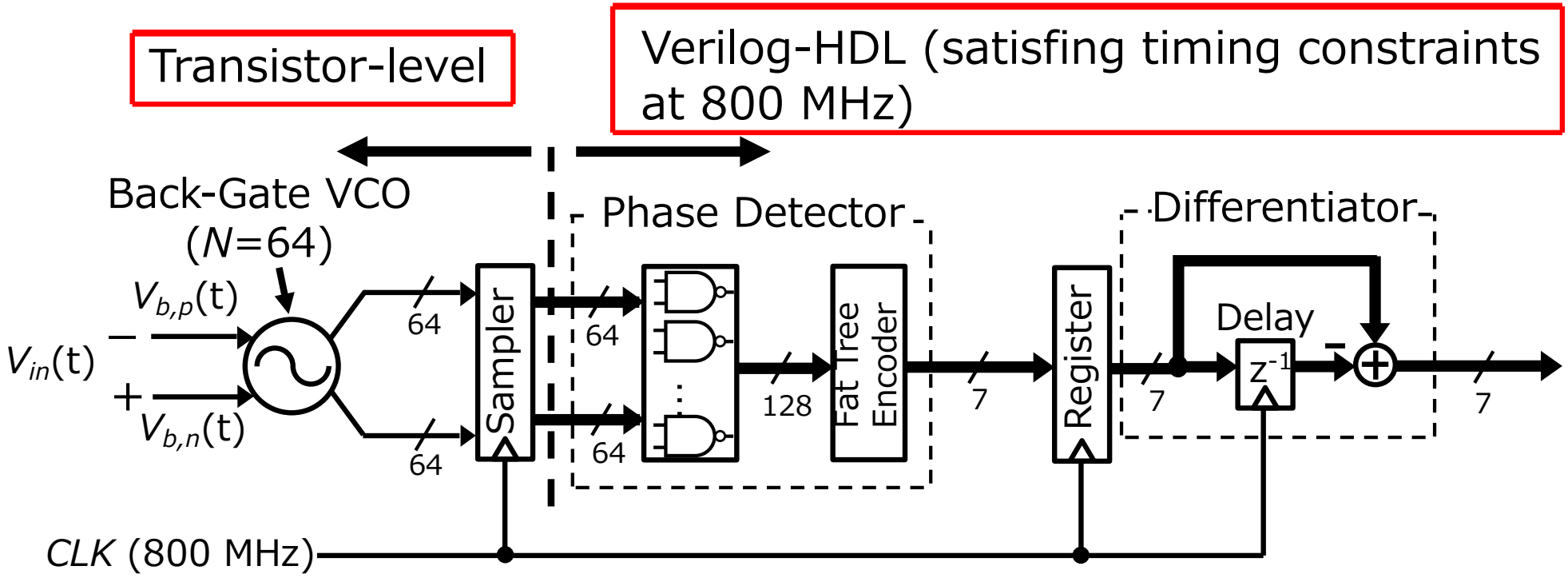
D.Lee, et al, IEEE Int.Midwest symp.circuit and systems, vol. 2, pp. Ⅱ-87-Ⅱ-90, Aug. 2002.

- Fat tree encoder can operate at higher sampling frequencies than a ROM-based encoder.
- Delay is an order of $\log_2(B_{in,en})$.
- Operating speed is improved by inserting pipling resisters into each stage.

$B_{in,en}$: Input bit width of encoder

Simulation

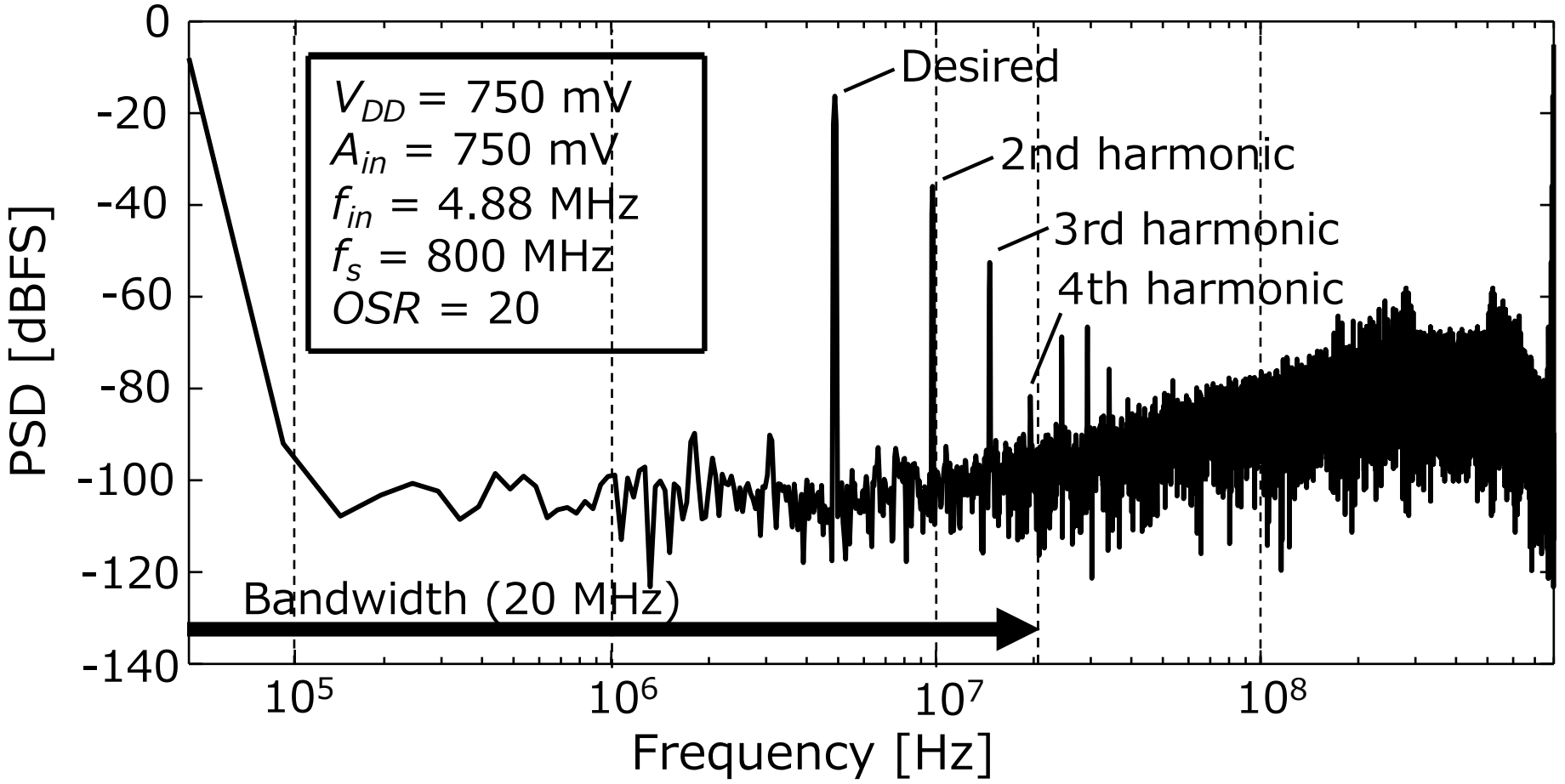
- Process: Renesas 65 nm SOTB CMOS
- Supply voltage: 750 mV
- Simulator: Synopsys VCS and XA



Input amplitude A_{in}[mV]	Input frequency f_{in} [MHz]	Input common voltage [mV]	Clook frequency f_s [MHz]	*OSR*	Sampling points
750	4.882	375	800	20	16384

SOTB : Silicon on thin buried oxide

Simulated Output Spectrum



- The SNR of the ADC was evaluated by the simulated output spectrum Achieved by FFT on MATLAB
- SNR (simulated) = 57.9 dB, SNR (theoretical) = 56.2 dB
- Nonlinearity of K_{vco} causes harmonics (SNDR = 19.7 dB)

$$\mathrm{SNR} \approx 6.02 \log_2(2A_{in}K_{VCO}N_{st}/f_s) + 2.61 + 30 \log \mathrm{OSR}\ [\mathrm{dB}]$$

K_{vco} = 89.3 MHz/V, number of VCO stage, N_{st} = 64

Comparision

	f_s [MHz]	BW [MHz]	SNR [dB]	SNDR [dB]	ENOB [bit]	P_{DD} [mW]	FoM [fJ/step]
TCAS-I'14 [2]	200	25.62	52.8	50.3	8.06	3.3	151.7
JSSC'17 [3]	1600	10.0	66.2	65.7	10.6	3.7	111
This work	800	20.0	57.9	18.7	2.81	2.7	105

$$FoM = \frac{P_{DD}}{2^{(\text{SNR-1.76})/6.02} \cdot 2BW} \qquad \text{ENOB} = \frac{SNDR\text{-}1.76}{6.02}$$

- Proposed ADC obtained the best FoM among the ADCs.
- SNDR was the lowest due to harmonics.

FoM: Figure of merit ENOB: Effective number of bits P_{DD}: Power consumption

Summary

- 800-MS/s ADC with a back-gate VCO and a fat tree encoder
  - All blocks consist of digital standard cells.
  - Back-gate VCO generates rail-to rail output signals, requiring no level conversion.
  - Phase detector using a fat tree encoder can operate at higher sampling frequencies than detectors based on counters.
  - Simulated SNR (57.9 dB) corresponds to the theoretical value (56.2 dB).
  - Obtained Best FoM among previously reported ADCs.