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# A 0.55 V Back-Gate Controlled Ring VCO for ADCs in 65 nm SOTB CMOS

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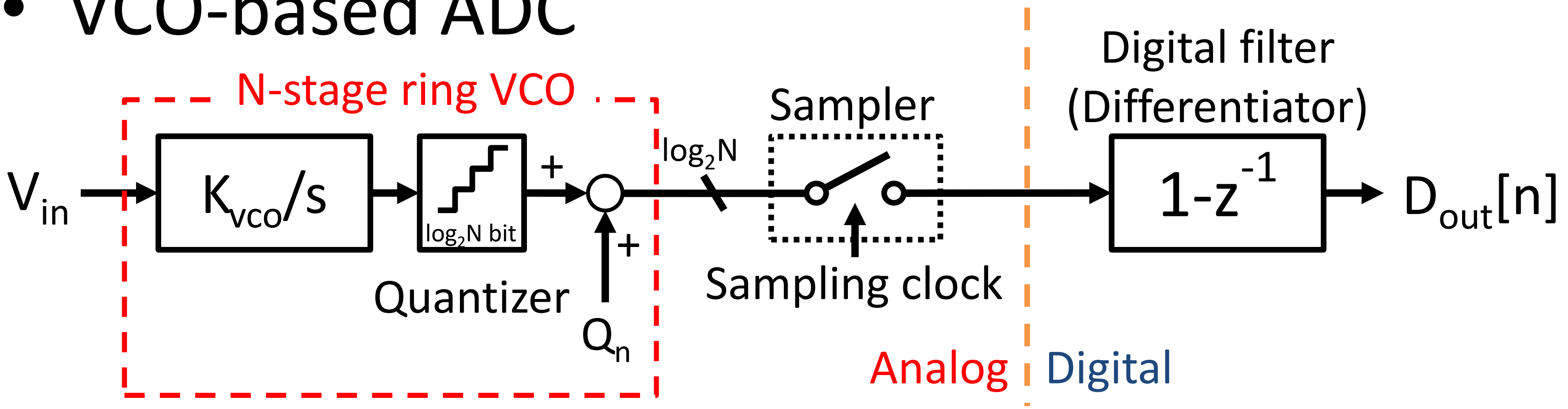
Microwaves for the Internet of Things

# Outline

- Introduction
- Requirements for ring VCO
- Conventional and Proposed Delay Cells
- Measurements
- Conclusion

# Introduction

- VCO-based ADC

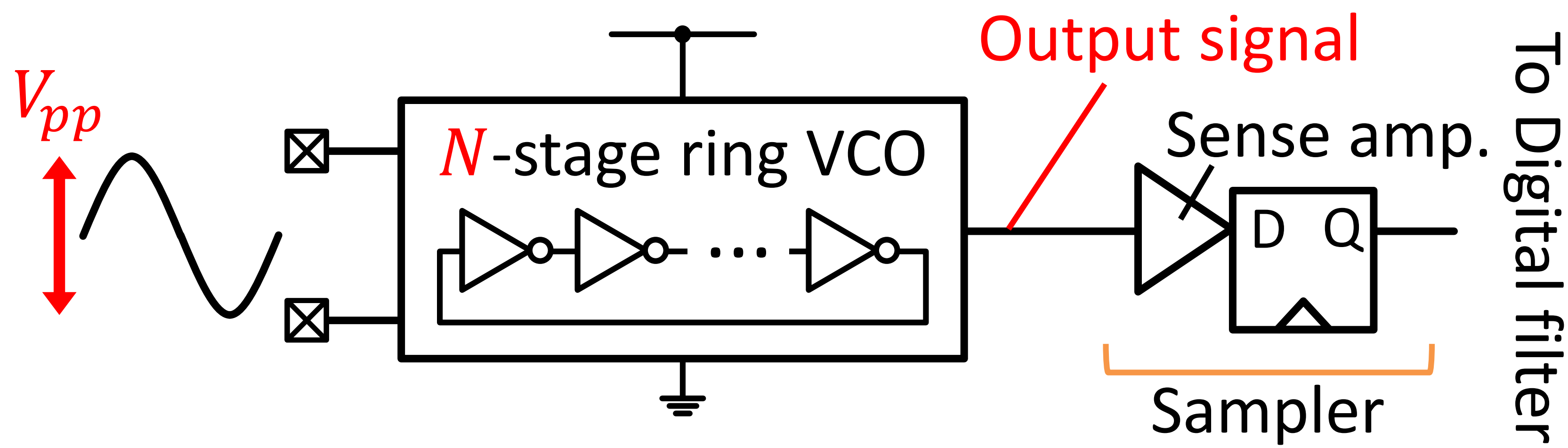



  - Digital-rich structure
  - High-speed sampling ( ~GHz )
  - High-pass noise shaping (as 1st-order DSM ADC)

$$D_{out}[n] = \underbrace{s^{-1}(1-z^{-1})}_{\approx f_s^{-1}} K_{VCO} V_{in} + \underbrace{(1-z^{-1})}_{\text{High-pass response}} Q_n$$

VCO: Voltage Controlled Oscillator, ADC: Analog to Digital Converter,
DSM: Delta Sigma Modulation

# Requirements for Ring VCO




- Low power

  VCO consumes 44% current in the ADC.

  Ref. J.Kim, S.H.Cho et.al. ISSCC 2011.

- Large control (input) range and more VCO stages

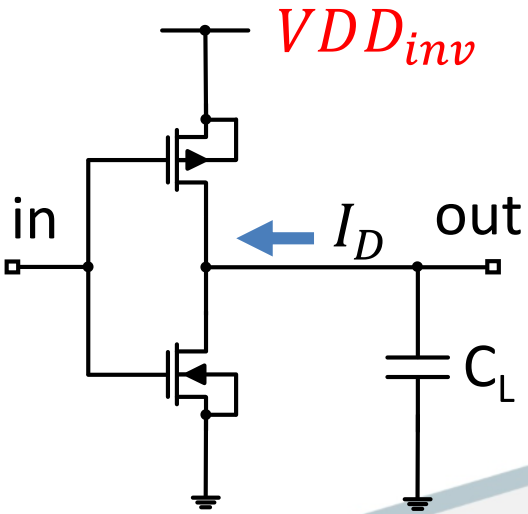
  $\mathrm{SQNR} \approx 6.02 \log_2(V_{pp} K_{VCO} N T_s) + 2.61 + 30 \log \mathrm{OSR}$ [dB]

- Rail-to-rail (GND to VDD) output signals

  Can eliminate sense amplifiers and low power consumption.

# Conventional Delay Cell

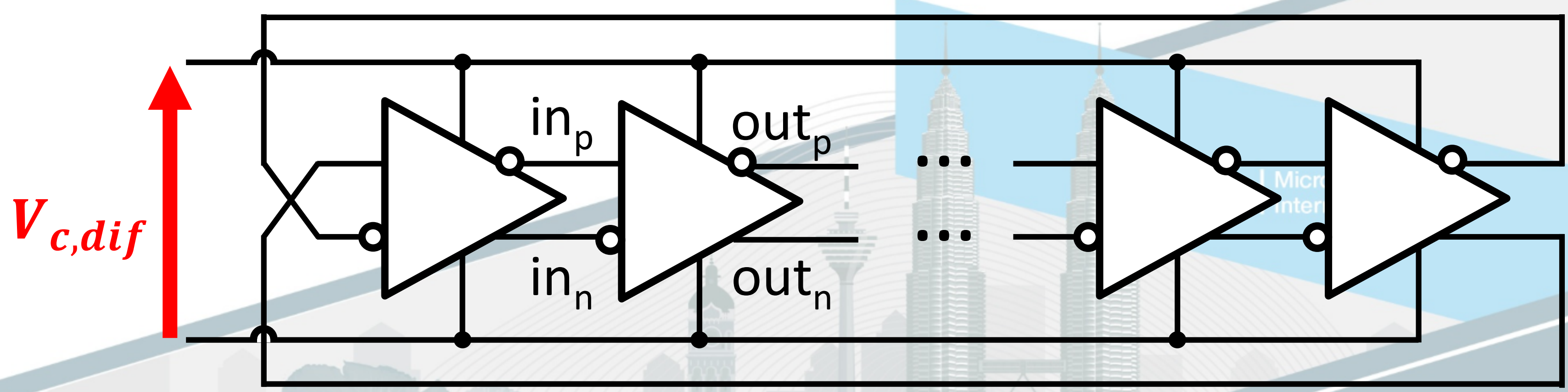
- Supply voltage controls the delay: $t_d$
  - $t_d = \frac{C_L VDD_{inv}}{|I_D|} \propto VDD_{inv}$




- Control voltage: $VDD_{inv}$
  - Single-ended
  - Narrow range due to saturation conditions.
- Output amplitude: $V_o$
  - $V_o = VDD_{inv}/2$
  - Small and not constant

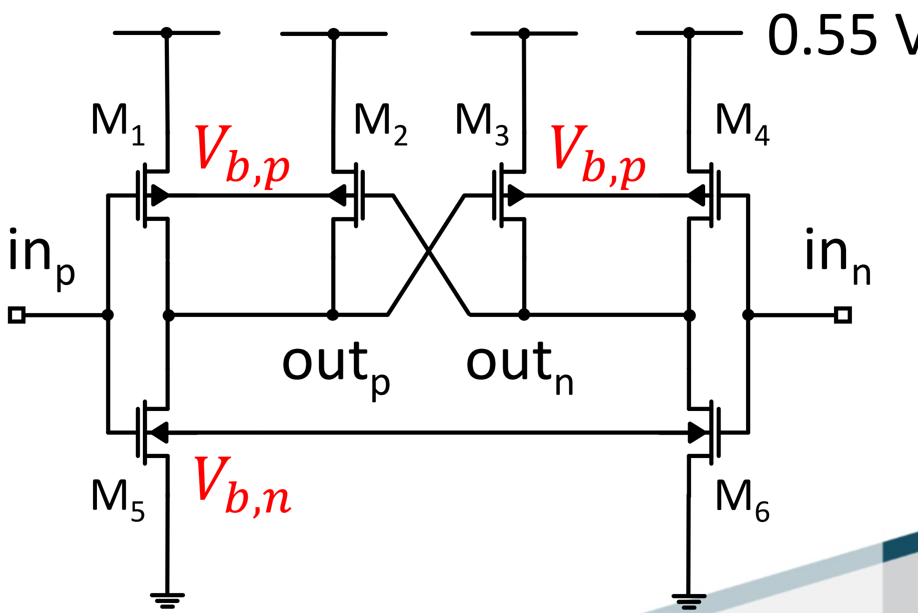
# Proposed Ring VCO

- Objectives
  - Low supply voltage ( 0.55 V )
  - Differential control: $V_{c,dif}$
  - 30 stages
  - Oscillation frequency < 600 MHz
  - Rail-to-rail (GND to VDD) output signals



# Proposed Delay Cell

- Back-gate controlled
  - $V_{b,p}, V_{b,n}$
- Differential control
  - $V_{c,dif} = V_{b,p} - V_{b,n}$
  - Wide range ( 2 x VDD )
- No tail current source
  - Low-voltage operation: 0.55 V
  - Rail-to-rail (GND–VDD) outputs

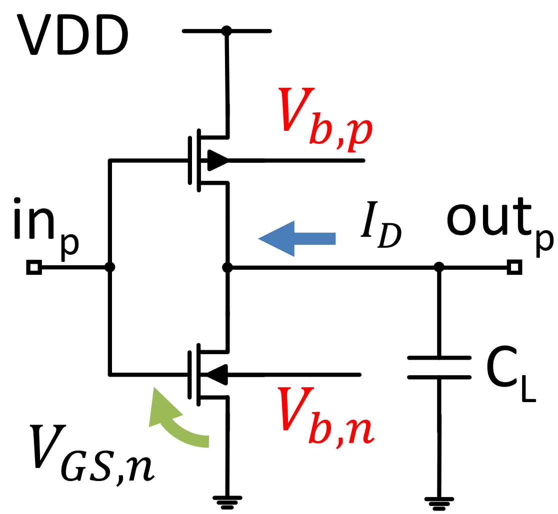



| | Width* [µm] | Length [nm] |
|---|---|---|
| $M_1,M_4$ | 1 x 12 | 65 |
| $M_2,M_3$ | 1 x 8 | 65 |
| $M_5,M_6$ | 0.5 x 20 | 65 |

* Unit width x fingers

# Back-Gate Controlled Delay

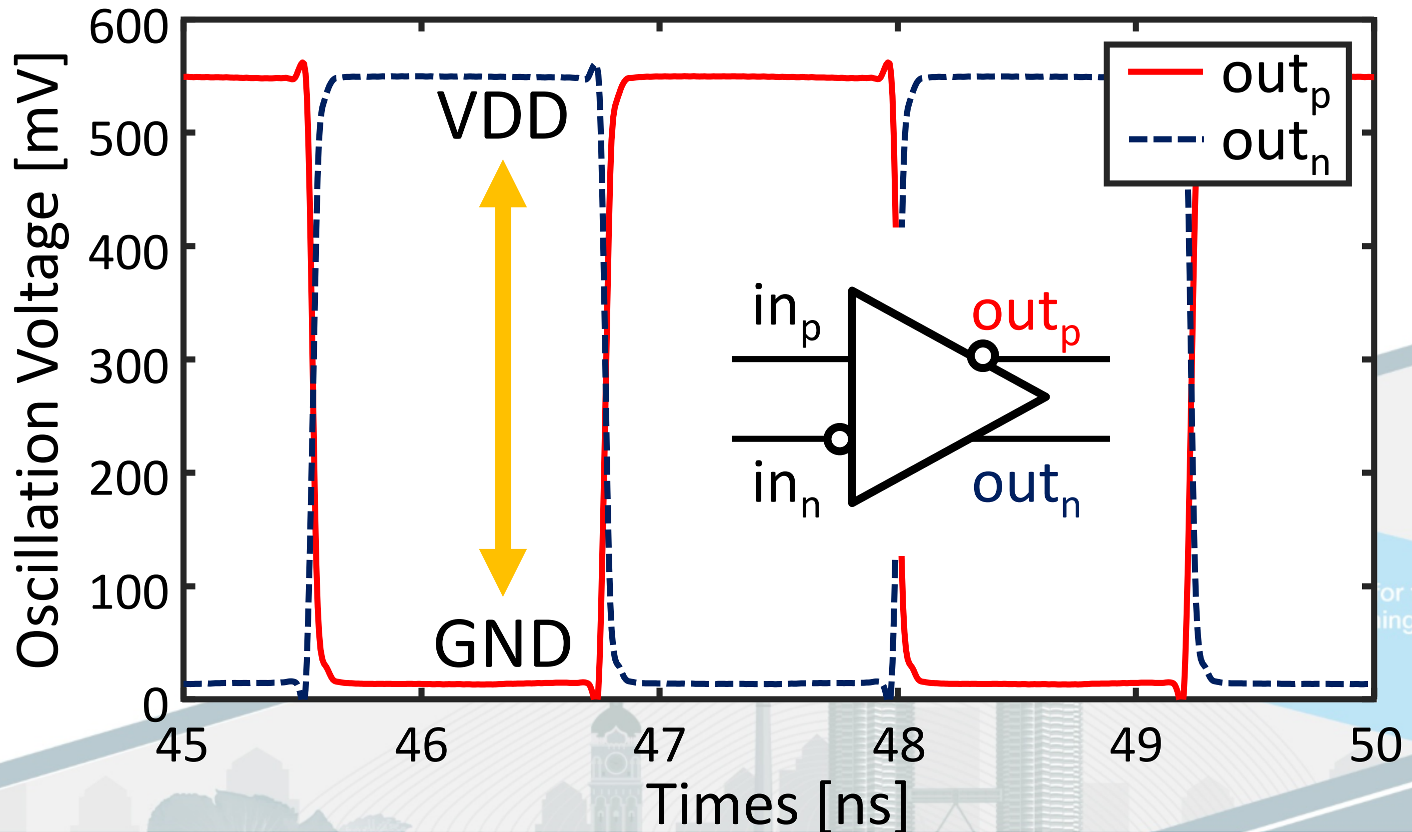
- Inverter delay $t_d$
  - $t_d = \frac{C_L VDD}{|I_D|} \propto |I_D|^{-1}$




- Inverter current $I_D$
  - $I_D = \frac{\beta_n}{2}\left(V_{GS,n} - V_{th,n}\right)^2, \beta_n = \mu_n C_{ox}\frac{W}{L}$
  - $V_{th,n} = V_{th,n0} + \gamma\left(\sqrt{|2\Phi_f + V_{s,n} - V_{b,n}|} - \sqrt{|2\Phi_f|}\right)$
  - Controlling $V_{b,n}$ and $V_{b,p}$ differentially leads to wider range of $I_D$.

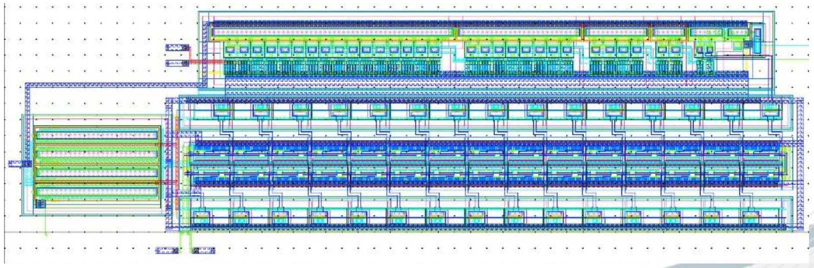
# Simulated Wave Forms

- VCO has rail-to-rail output signals
  - Can be sampled by digital latch in VCO-based ADC.

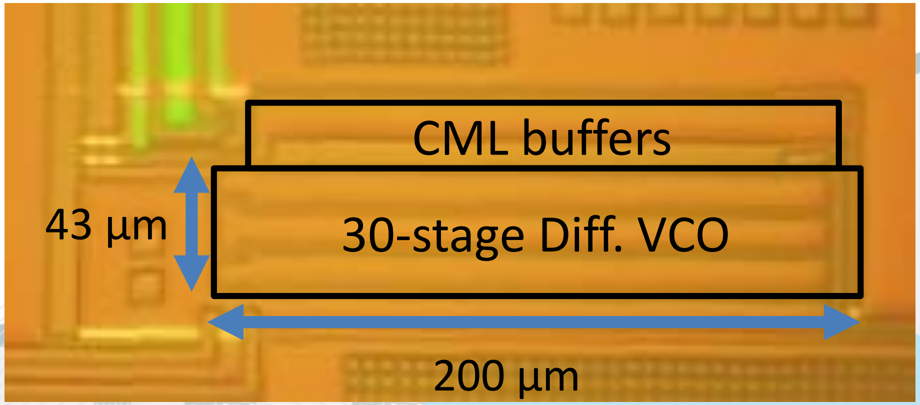


# Fabricated Ring VCO

- VCO is fabricated in SOTB 65nm CMOS
  - VCO core: 43 x 200 μm$^2$
  - Supply voltage: 0.55 V
- CML buffers are used only for measurements



Layout

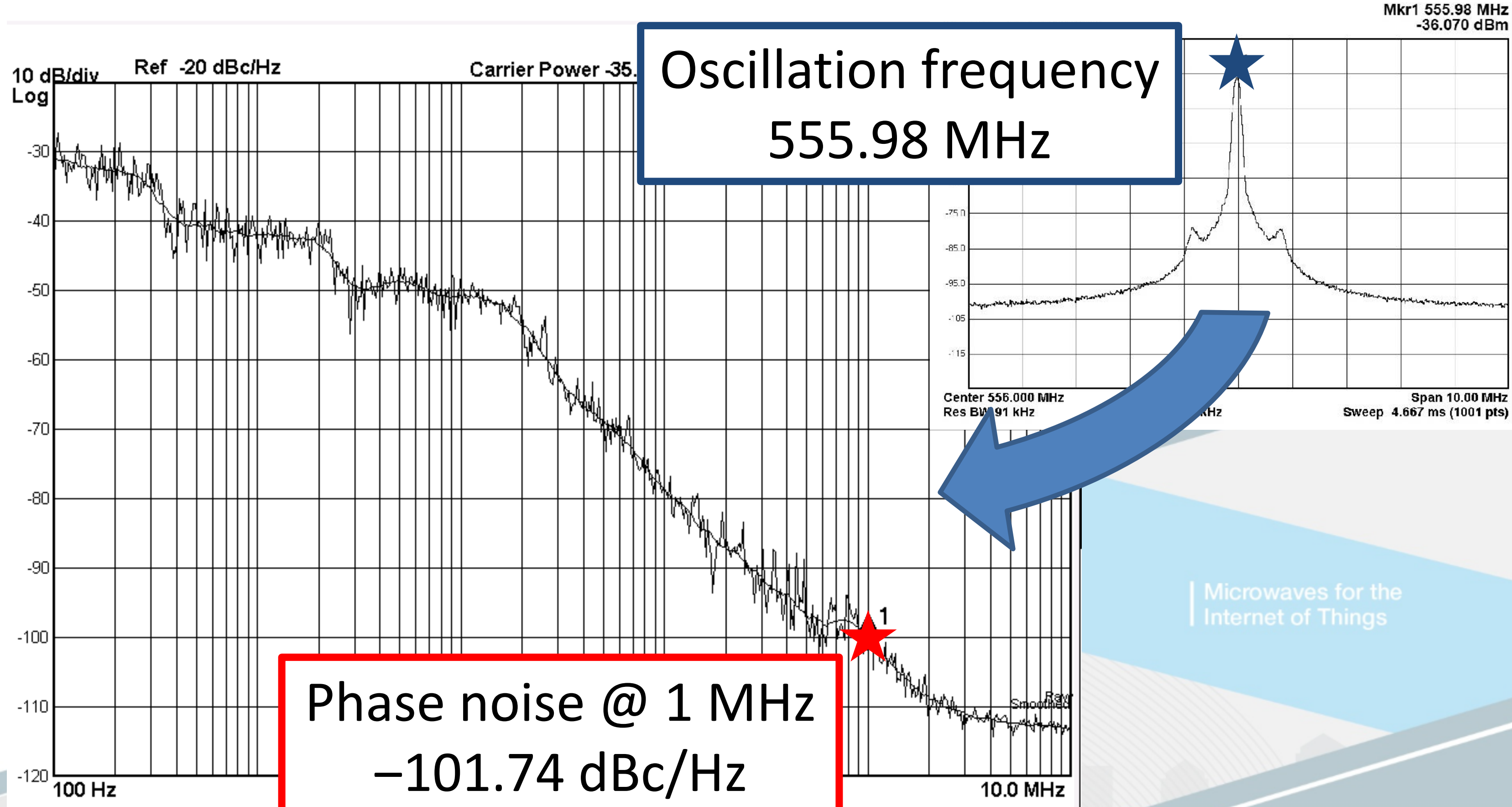



Chip photo

SOTB: Silicon-On-Thin-Box

# Measured Spectrum

- Spectrum and phase noise
  - Control voltage: $V_{c,dif} = V_{b,p} - V_{b,n} = -0.55$ [V]

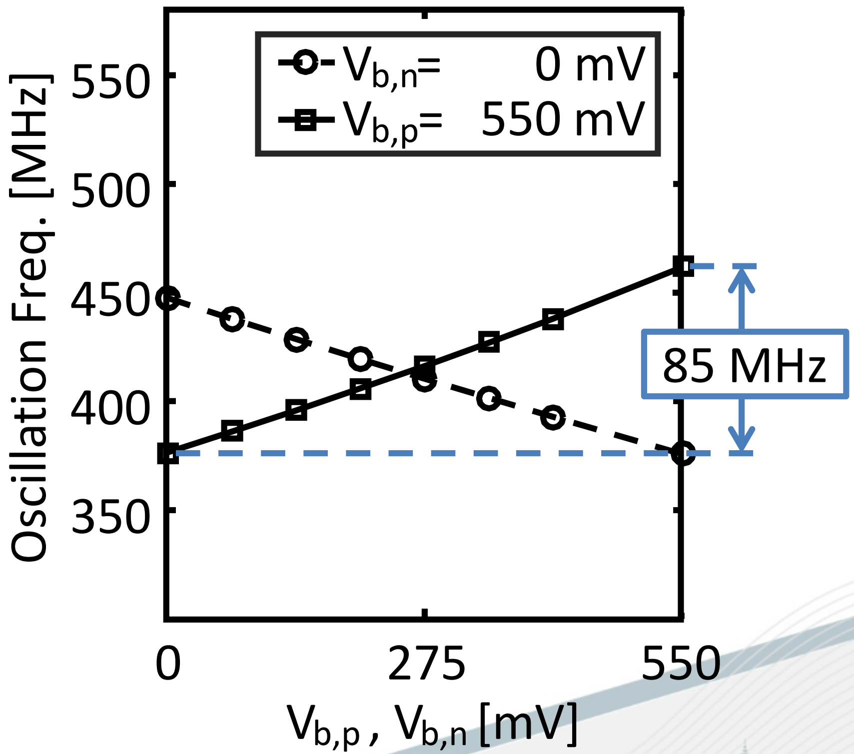


# Measured Results

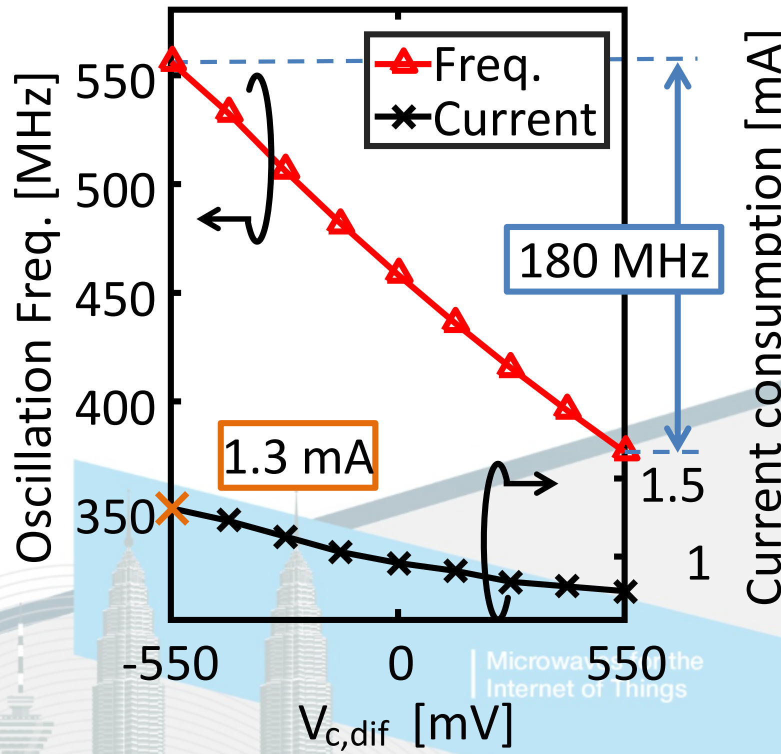


- Oscillation frequency and current vs. control voltages

Single-ended control




Differential control




Differential control doubles the tuning range

# Performance Summary

| Ref. | CMOS tech. | $P_{DC}$ [mW] | Control range [V] | Tuning range [MHz] | Rail-to-rail output | FoM [dBc/Hz] |
|---|---|---|---|---|---|---|
| This work | 65 nm | 0.72 | -0.55 ~ 0.55* | 376 ~ 556 | yes | -158.0 |
| [1] | 90 nm | 1.16 | 0.0 ~ 0.5 | 160 ~ 2500 | no | -153.4 |
| [5] | 90 nm | 0.087 | 0.0 ~ 0.6 | 40 ~ 771 | no | -157.4 |
| [6] | 65 nm | 10.0 | 0.0 ~ 0.8 | 500 ~ 1000 | yes | -157.0 |

* Differentially controlled

$$FoM = L\{\Delta\omega\} + 10\log_{10}(P_{DC}) - 20\log_{10}\left(\frac{\omega_0}{\Delta\omega}\right)$$

$L\{\Delta\omega\}$: Phase noise at $\Delta\omega$ [Hz] offset, $P_{DC}$: Power consumption, $\omega_0$: Oscillation frequency



VCO type: [1] PMOS back-gate controlled VCO
[5] Supply-voltage controlled DCO
[6] Current-bias controlled VCO

# Conclusion

- Differentially back-gate VCO for ADCs
- Low supply voltage operation ( 0.55 V )
- Rail-to-rail ( GND to VDD ) output signals
- Larger control voltage range ( 2 x VDD )
- Best FoM among low-voltage ring VCOs. ( -158.0 dBc/Hz )

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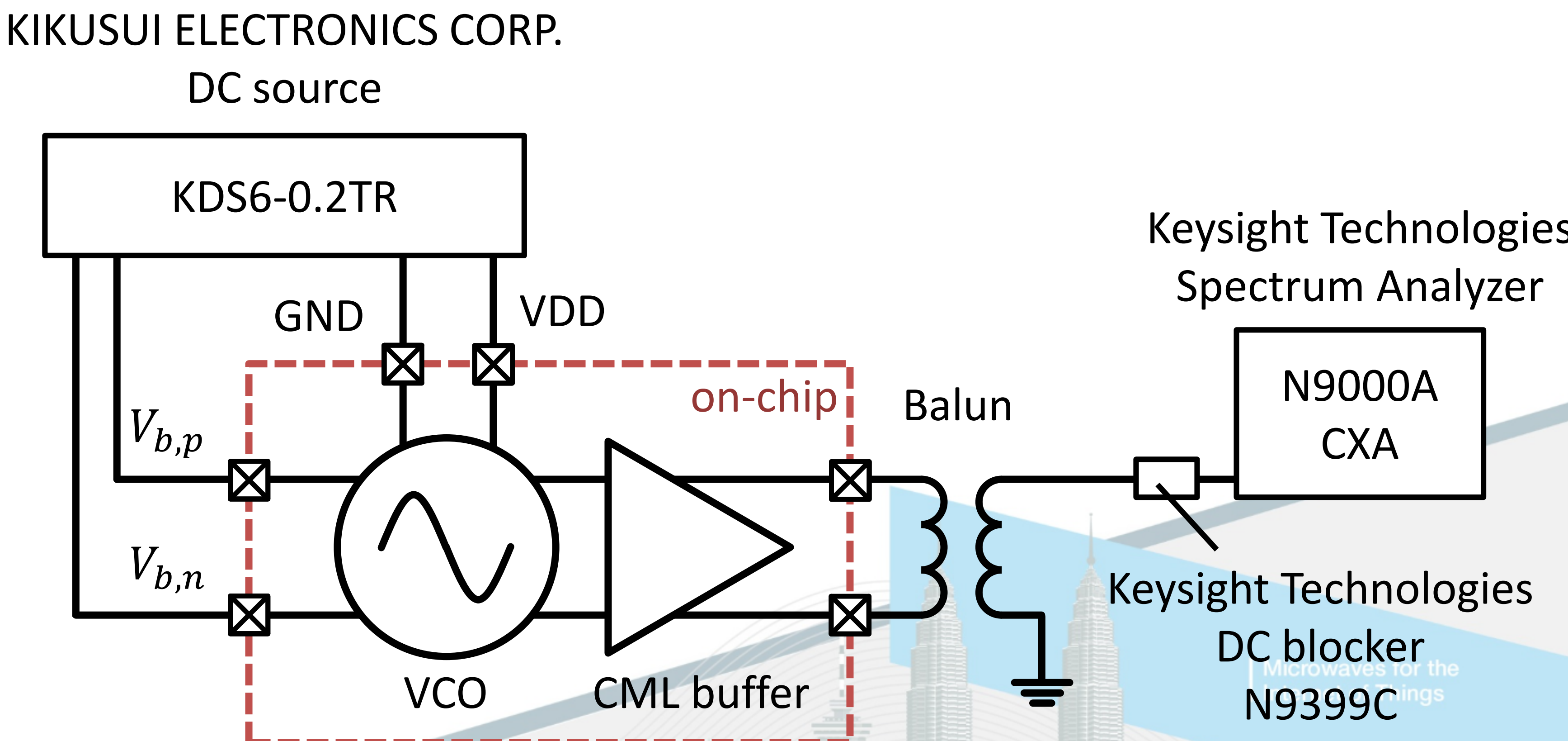
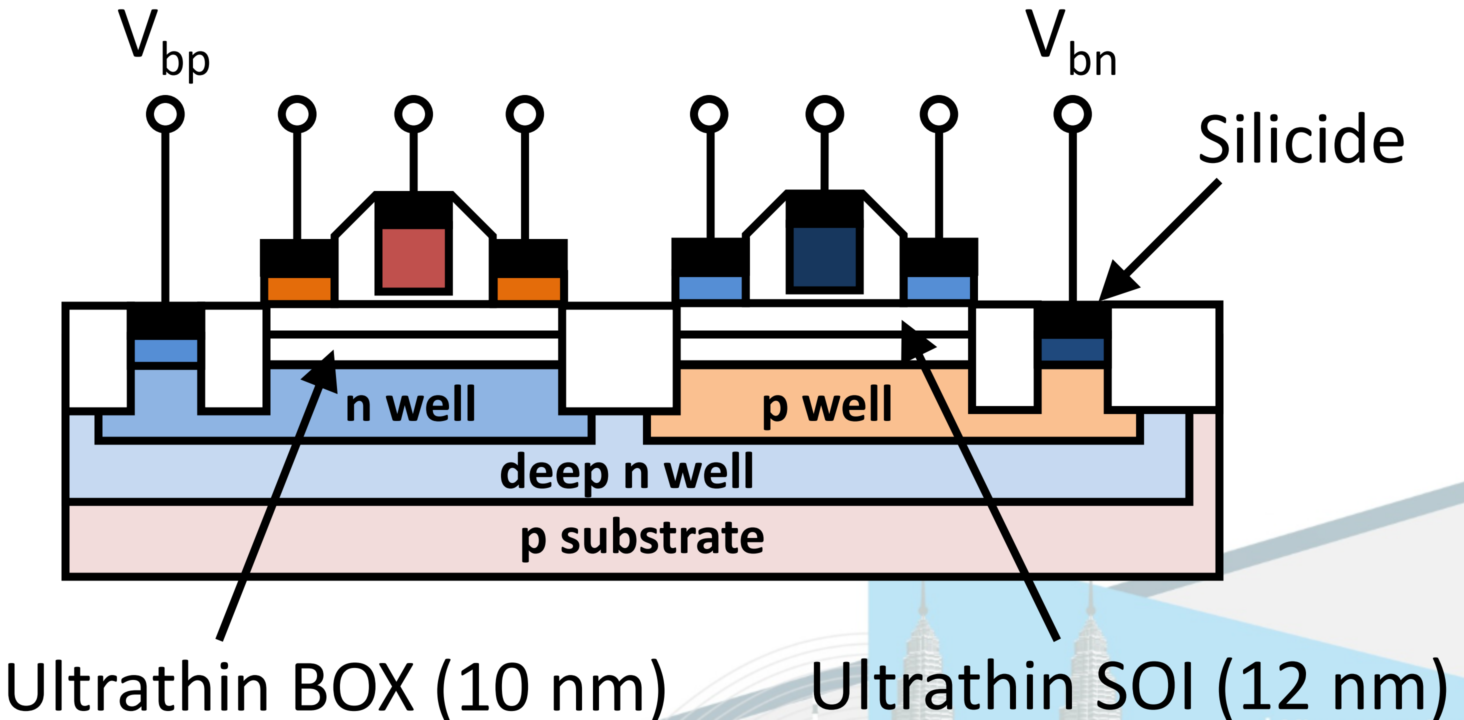
- Keysight Technologies Japan, Ltd.

# Measurement System



# SOTB Process

- Schematic cross section of SOTB CMOS




Ref. S. Kamohara et al., 2014 VLSI Tech.